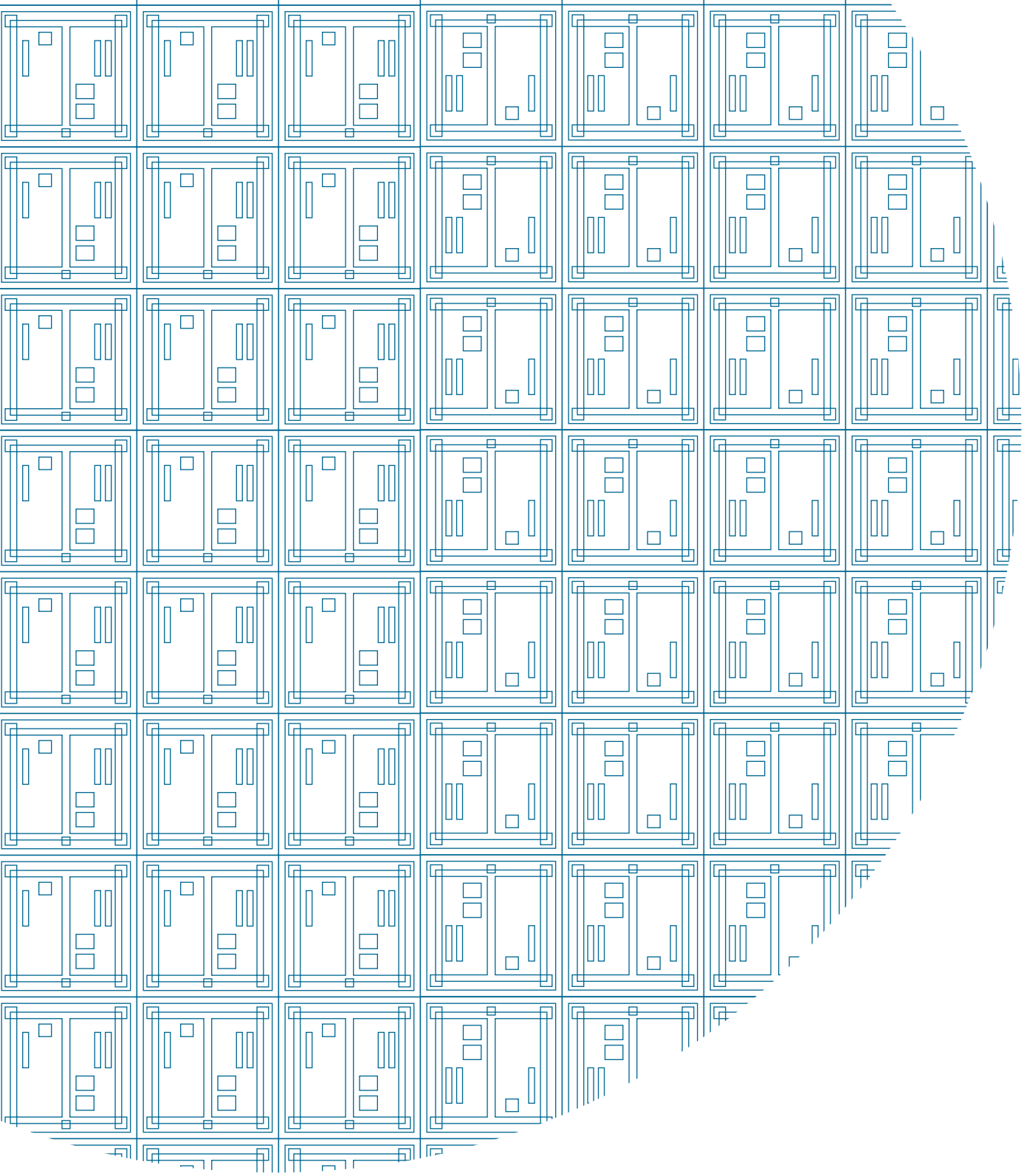
ALTERA®

Altera Product Catalog 2007



The Programmable Solutions Company®

Design with confidence

One thing hasn't changed since Altera created the world's first reprogrammable logic device more than 20 years ago: a commitment to innovation—ours and yours.

Your success depends on differentiating your products, getting to market first, and increasing profitability. We're committed to giving you the resources to design your systems with confidence through a product portfolio that includes:

- The industry's most advanced FPGA, CPLD, and structured ASIC technologies
- Versatile embedded processors
- Optimized intellectual property (IP) cores
- A fully integrated software development tool
- Off-the-shelf development kits

Turn the page to start learning more about Altera® programmable solutions, or visit www.altera.com.

Contents

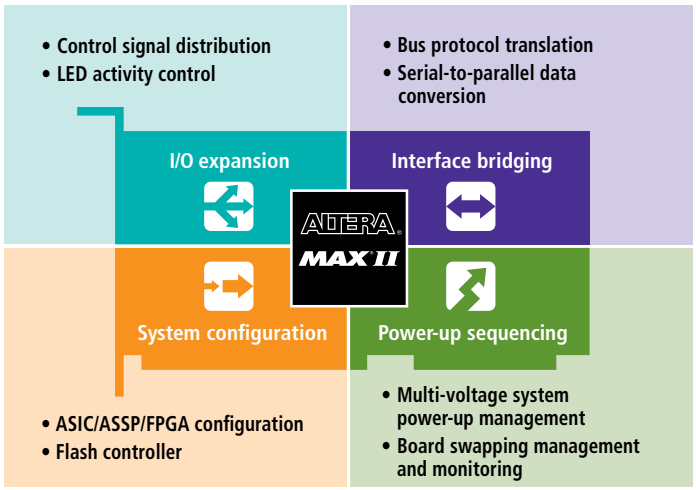
MAX CPLD series

Altera's market-leading MAX® series of CPLDs are world-class, low-cost devices designed for virtually any digital control function. As non-volatile, single-chip solutions, MAX CPLDs are easy to incorporate into your system. With the devices, you can solve board-level issues such as insufficient I/O pins on a processor, manage the power-up sequence or configuration of other more complex devices, or inexpensively convert incompatible interfaces (a.k.a. "glue logic"). Designed to be hassle-free with intuitive device behavior and software, MAX CPLDs give you the freedom to focus on your more complex design challenges.

Key features

- Low cost
- Zero power
- Small packages
- Instant-on and non-volatile
- In-system programmability (ISP)
- Free Quartus® II Web Edition software support
- Free ModelSim®-Altera Web Edition software support

MAX II application areas



MAX® II

The market's lowest-cost CPLDs

MAX II devices are based on a ground-breaking architecture that combines the best of FPGAs and CPLDs. The performance and density benefits of a four-input look-up table (LUT) architecture are merged with the usability and cost advantages of a non-volatile architecture. The result? A first-in-its-class, new architecture that sets standards for cost, power consumption, performance, and density for CPLDs.

With MAX II CPLDs, you can reduce your system costs by integrating a larger amount of control logic into a single device. This instant-on, non-volatile device family targets general-purpose control logic applications. With the introduction of its power-down capability and ultra-small packages, these benefits are also available for portable applications requiring a zero-power solution. MAX II CPLDs are ideal for four key applications: I/O expansion, interface bridging, system configuration, and power-up sequencing.

MAX II family features summary

Cost-optimized architecture	Revolutionary MAX II architecture delivers four times the density at half the price of competing CPLDs.
Low power	Reduces power consumption and increases system reliability.
Highest-density CPLDs	Implements more applications in a single, low-cost device.
Small packages	Integrates on average 50 percent more user I/O pins and logic per board area (mm2) than competing CPLDs with 0.5-mm pitch BGA packages.
Non-volatile and instant-on functionality	Reduces system cost and board space with a single-chip solution.
User flash memory	Minimizes system cost and chip count by integrating discrete serial or parallel non-volatile storage onto MAX II devices.
Real-time ISP	Reduces maintenance costs by enabling updates while the device is in operation.
MultiVolt core	Operates with a 1.8-, 2.5-, or 3.3-V power supply, minimizing power rails and simplifying board design.
MultiVolt I/O interface	Interfaces seamlessly to other devices at 1.5-, 1.8-, 2.5-, or 3.3-V logic levels.
Parallel flash loader	Simplifies board management by using MAX II devices to configure external non-JTAG-compliant flash devices.

MAX®

General-purpose CPLDs

Altera's 3.3-V MAX 3000A devices are cost-optimized for high-volume applications, while the 5.0-, 3.3-, and 2.5-V MAX 7000 families offer world-class, high-performance solutions for a broad array of applications.

The non-volatile, EEPROM-based MAX 3000A and MAX 7000 families provide instant-on capability and offer densities from 32 to 512 macrocells. These devices support ISP and can be easily reconfigured in the field.

MAX 3000A family features summary

Low price per macrocell	Ideal for low-cost, high-volume applications.
4.5-ns propagation delays	Provides fast system performance.
5.0-V tolerant I/O pins	Inherently interfaces to 5.0-V devices.
Commercial and industrial temperature	Reduces overall system cost for temperature-sensitive applications.

MAX 7000 family features summary

4.5-ns propagation delays	Provides fast system performance.
Support for advanced I/O standards	Supports GTL+ and SSTL-2/-3 I/O standards (MAX 7000B CPLDs).
Programmable power-saving mode	Reduces power consumption by over 50 percent.
Commercial, industrial, and extended temperatures	Provides support for all environmental conditions.

MAX CPLD series package and I/O matrix

Device available in commercial temperature. Contact Altera for industrial temperature.

Device available in commercial and industrial temperatures.

Device available in commercial and industrial, and qualified to extended temperatures.

36 Number indicates available user I/O pins.

Vertical migration (Same V_{CC}, GND, ISP, and input pins).

		MAX II 3.3 V, 2.5 V, 1.8 V				MAX 3000A 3.3 V					MAX 7000AE 3.3 V				
		EPM240/G	EPM570/G	EPM1270/G	EPM2210/G	EPM3032A	EPM3064A	EPM3128A	EPM3256A	EPM3512A	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Density and speed	**Macrocells**[1]	192	440	980	1,700	32	64	128	256	512	32	64	128	256	512
	Logic elements (LEs)	240	570	1,270	2,210	–	–	–	–	–	–	–	–	–	–
	Pin-to-pin delay (ns)	4.7, 6.2, 7.6	5.5, 7.1, 8.8	6.3, 8.2, 10.1	7.1, 9.2, 11.3	4.5, 7.5, 10	4.5, 7.5, 10	5.0, 7.5, 10	7.5, 10	7.5, 10	4.5, 7.5, 10	4.5, 7.5, 10	5.0, 7.5, 10	5.5, 7.5, 10	7.5, 10, 12
PLCC (L)[2]	**44-pin**					34	34				36	36			
	84-pin												68		
TQFP (T)[3]	**44-pin**					34	34				36	36			
	100-pin	80	76				66	80				68	84	84	
	144-pin		116	116				96	116				100	120	120
PQFP (Q or R)[4]	**208-pin**								158	172				164	176
BGA (B)[5]	**256-pin**														212
FBGA (F)[6]	**100-pin**	80	76									68	84	84	
	256-pin		160	212	204			98	161	208			100	164	212
	324-pin				272										
MBGA (M)[7]	**100-pin**	80	76												
	256-pin		160	212											

1 Typical equivalent macrocells for MAX II devices
2 Plastic J-lead chip carrier
3 Thin quad flat pack
4 Plastic quad flat pack
5 Ball-grid array (1.27 mm)
6 FineLine BGA (1.0 mm)
7 Micro FineLine BGA (0.5 mm)

MAX CPLD series features

		MAX II CPLDs 3.3 V, 2.5 V, 1.8 V				MAX 3000A CPLDs 3.3 V					MAX 7000AE CPLDs 3.3 V				
		EPM240/G	EPM570/G	EPM1270/G	EPM2210/G[1]	EPM3032A	EPM3064A	EPM3128A	EPM3256A	EPM3512A	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Features	User flash memory (Kbit)	8				–					–				
	Boundary scan JTAG	✓				✓					✓				
	JTAG ISP	✓				✓					✓				
	Fast input registers	✓				–					✓				
	Programmable register power-up	✓				–					✓				
	Programmable ground pins	✓				–					✓				
	Open-drain outputs	✓				✓					✓				
	Programmable pull-up resistors	✓				–					–				
	Bus hold	✓				–					–				
	JTAG translator	✓				–					–				
	Real-time ISP	✓				–					–				
	0.5-mm BGA packages	✓				–					–				
Core voltage and I/O options	Core voltage (V)	1.8				3.3					3.3				
	MultiVolt core (V)	3.3, 2.5, 1.8				–					–				
	MultiVolt I/O (V)	3.3, 2.5, 1.8, 1.5				5.0, 3.3, 2.5					5.0, 3.3, 2.5				
	I/O power banks	2	2	4	4	1					1				
	Maximum I/O pins	80	160	212	272	34	66	98	161	208	36	68	100	164	212
	Maximum output enables	80	160	212	272	6	6	6	6	10	6	6	6	6	10
	Transistor-to-transistor logic (TTL) (5.0-V tolerance)	–	–	✓[2]	✓[2]			✓					✓		
	LVTTL/LVCMOS	✓						✓					✓		
	32-bit, 66-MHz PCI compliant	–	–	✓	✓			–					–		
	GTL+/SSTL-2, SSTL-3, all class I and class II	–						–					–		
	Schmitt triggers	✓						–					–		
	Programmable slew rate	✓						✓					✓		
	Programmable drive strength	✓						–					–		

[1] There are no 0.5mm BGA packages available

[2] An external series resistor must be used for 5.0-V tolerance

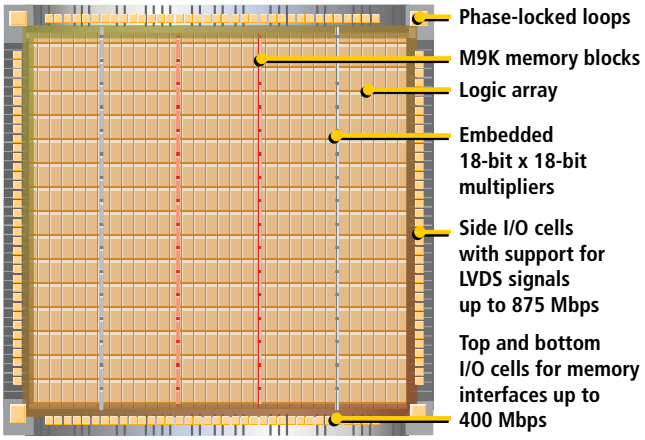
Cyclone low-cost FPGA series

For your cost-sensitive, high-volume applications, Altera offers our Cyclone® FPGA series —the industry's only FPGAs designed from the ground up for low cost. Each family member is individually optimized for cost and delivers a high-volume solution that's competitive with ASICs and ASSPs. This series of FPGAs—including the 65-nm Cyclone III, 90-nm Cyclone II, and 130-nm Cyclone families—delivers a customer-defined feature set, industry-leading performance, and the lowest power consumption.

Key features

- The industry's lowest-cost FPGAs
- High-performance digital signal processing (DSP)
- Low-cost embedded processing
- Free Quartus II Web Edition software support
- Free ModelSim®-Altera Web Edition software support

Cyclone III floorplan



Cyclone III 65-nm low-cost FPGAs

Cyclone III FPGAs, the newest offering in this series of low-cost devices, features an unprecedented combination of low power, high functionality, and low cost to deliver more, sooner, and for less—even for your most cost-sensitive, high-volume applications. Built on Taiwan Semiconductor Manufacturing Company's (TSMC's) 65-nm low power (LP) process technology, Cyclone III was designed to provide customers with the flexibility and application-optimized features to enable the highest levels of design possibilities and productivity while meeting the most stringent cost and power budgets. What's more, this can be accomplished without the high NRE costs associated with ASICs.

Because our engineers defined, designed, and developed Cyclone III FPGAs with customer feedback in mind, the devices provide the ideal features to meet your needs. The logic-, memory-, and DSP-rich architecture enables you to enhance system integration for your applications. From video and image processing to displays and wireless applications, the opportunities for Cyclone III devices are unlimited.

Cyclone III family features summary

Cost-optimized architecture	Offers from 5,136 to 119,088 LEs—70 percent more than the Cyclone II FPGA family for enhanced system integration.
Low-power architecture	Altera's innovative power-saving features and TSMC's 65-nm LP process technology come together to minimize both standby and dynamic power consumption. Quartus II design software provides a power-aware design flow to enable optimization for minimal power usage. Compared to Cyclone II FPGAs, Cyclone III devices deliver up to 50 percent lower power.
Embedded memory	Up to 4 Mbits of embedded memory for memory-intensive applications such as video line buffers.
Embedded multipliers	Up to 288 dedicated 18-bit x 18-bit multipliers with 260-MHz performance for high-bandwidth parallel processing applications.
External memory interfaces	Support for high-speed external memory interfaces including DDR, DDR2, SDR SDRAM, and QDR II SRAM at up to 400 megabits per second (Mbps). The autocalibrating external memory interface PHY feature eases timing closure and eliminates variations over process, voltage, and temperature (PVT).
Robust clock management	Up to 4 phase locked loops (PLLs) per device with 5 outputs per PLL providing up to 20 global clocks. Supports dynamic reconfiguration for frequency and phase changes.
Differential signaling	Supports up to 875-Mbps receive and 840-Mbps transmit LVDS signaling. Ability to use reduced swing differential signaling (RSDS), LVDS, and point-to-point differential signaling (PPDS) without external resistors.
Commodity parallel configuration	Support for low-cost configuration options.
Remote system upgrade	Allows storage of multiple configuration images in a single configuration device for field upgrades. Automatic error correction circuitry restores factory image if error detected.

Cyclone III family features summary (continued)

Automatic SEU detection circuitry	Features automatic single event upset (SEU) detection circuitry utilizing 32-bit cyclic redundancy check (CRC).
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support that ensures proper device operation independent of the power-up sequence.
MegaCore® IP library	Shorten design time using a broad portfolio of more than 200 Altera and partner intellectual property (IP) cores. Altera IP can be evaluated in hardware before purchase.
Nios® II embedded processor support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors to reduce cost and increase flexibility. Nios II soft processor support for Cyclone III FPGAs offers over 100-DMIPS performance.
Free software support	The free, downloadable Quartus II Web Edition software supports the entire Cyclone III family with its unprecedented combination of low power, high functionality, and low cost. Quartus II Web Edition software offers productivity and performance features including TimeQuest timing analysis, PowerPlay power optimization, and SOPC Builder, providing the fastest path to design completion for Cyclone III FPGAs.

Cyclone™ II

90-nm low-cost FPGAs

As the second-generation offering in the Cyclone series, the Cyclone II FPGA family offers more density and features at dramatically lower costs, compared with its predecessor. Based on a 1.2-V, 90-nm, low-k dielectric process, the devices include dedicated DSP circuitry for very low-cost DSP solutions. If you're implementing Nios II embedded processors on Cyclone II FPGAs, you can create cost-effective processing solutions for price-sensitive and compute-intensive applications.

Cyclone II family features summary

Cost-optimized architecture	Offers from 4,608 to 68,416 LEs—three-and-a-half times the density of first-generation Cyclone FPGAs—and the lowest cost per LE.
Embedded memory	Up to 1.1 Mbits of RAM via 4,608-bit memory blocks capable of 250-MHz performance. Support for multiple configurations, including true dual-port and single-port RAM, ROM, and first-in first-out (FIFO) buffers.
Embedded multipliers	150 18-bit x 18-bit embedded multipliers running at 250 MHz that can implement common DSP functions such as finite impulse response (FIR) filters and fast Fourier transforms (FFTs). Each 18-bit x 18-bit multiplier can be configured as two independent 9-bit x 9-bit multipliers.
Nios II embedded processor support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors to reduce cost and increase flexibility. Nios II soft processor support for Cyclone II FPGAs offers over 100-DMIPS performance.
Differential and single-ended I/O standards support	Support for LVTTL, LVCMOS, PCI, PCI-X, PCI Express[1], SSTL, and high-speed transceiver logic (HSTL) single-ended I/O standards. Differential signaling support for LVDS (805 Mbps receiving and 640 Mbps transmitting), mini-LVDS, RSDS, LVPECL, SSTL, and HSTL system interfaces.
External memory interfaces	Dedicated interfaces supporting external memory devices at 167 MHz for integration with external SDR, DDR, DDR2 SDRAM, and QDR II SRAM devices. Altera offers DDR, DDR2, and QDR II memory controller MegaCore functions free with Quartus II software subscriptions.
Clock management circuitry	16 low-skew, global clock networks span the entire device, fed by 16 dedicated input clock pins. Four PLLs provide complete system clock management on and off chip. Each PLL has three output taps, and features programmable bandwidth, programmable duty cycle, spread-spectrum clocking, lock detection, and frequency synthesis with phase-shifting capabilities.
On-chip termination	Single-ended on-chip termination support for driver impedance matching and series termination eliminates the need for external resistors, improves signal integrity, and simplifies board design.
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support that ensures proper device operation independent of the power-up sequence.
Automatic SEU detection circuitry	Features automatic SEU detection circuitry utilizing 32-bit CRC.

[1] Requires external PHY device

Cyclone™

130-nm low-cost FPGAs

Cyclone devices provide application-focused features such as embedded memory, external memory interfaces, and clock management circuitry at price points optimal for high-volume applications.

Cyclone family features summary

Cost-optimized architecture	Offers from 2,910 to 20,060 LEs; built for low cost.
Embedded memory	288 Kbits of RAM through 4,608-bit memory blocks that can be configured to support a wide range of operation modes including RAM, ROM, FIFO buffers, and single-port and dual-port modes.
Nios II embedded processor support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors to reduce cost and increase flexibility.
Single-ended I/O support	Supports a variety of single-ended I/O interface standards, such as the 3.3-V, 2.5-V, 1.8-V, LVTTL, LVCMOS, SSTL, and PCI standards needed for today's systems.
External memory interfaces	Dedicated external memory interfaces that allow you to integrate external SDR and DDR SDRAM devices into complex system designs without degrading data access performance.
Differential I/O support	Support for 129 LVDS and RSDS channels with 640-Mbps LVDS data rates and 311-Mbps RSDS data rates.
Clock management circuitry	Features up to two programmable PLLs and eight global clock lines that provide robust clock management and frequency synthesis capabilities enabling on- and off-chip system clock management. PLLs offer advanced features such as frequency synthesis, programmable phase shift, programmable delays, and external clock output.
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support that ensures that Cyclone devices operate no matter how the system is powered up.
Automatic SEU detection circuitry	Utilizes 32-bit CRC to minimize radiation problems.

EP1 EP2 EP3

Cyclone FPGA series comparative table

Device	LEs	Embedded RAM blocks[1]	RAM Kbits	18-bit x 18-bit multipliers	PLLs	Clock outputs per PLL	I/O banks	Max LVDS channels[2]
EP1C3	2,910	13	58	-	1	3	4	34
EP1C4	4,000	17	76	-	2	3	4	129
EP2C5	4,608	26	119	13	2	3	4	61
EP3C5	5,136	46	414	23	2	5	8	62
EP1C6	5,980	20	90	-	2	3	4	72
EP2C8/A	8,256	36	165	18	2	3	4	75
EP3C10	10,320	46	414	23	2	5	8	62
EP1C12	12,060	52	234	-	2	3	4	103
EP2C15A	14,448	52	239	26	4	3	8	128
EP3C16	15,408	56	504	56	2	5	8	128
EP1C20	20,000	64	288	-	4	3	4	129
EP2C20/A	18,752	52	239	35	4	3	8	128
EP3C25	24,624	66	594	66	4	5	8	71
EP2C35	33,216	105	483	35	4	3	8	201
EP3C40	39,600	126	1,134	126	4	5	8	215
EP2C50	50,528	129	594	86	4	3	8	189
EP3C55	55,856	260	2,340	156	4	5	8	151
EP2C70	68,416	250	1,152	150	4	3	8	257
EP3C80	81,264	305	2,745	244	4	5	8	169
EP3C120	119,088	432	3,888	288	4	5	8	221

1 Cyclone and Cyclone II have 4-Kbit RAM blocks; Cyclone II has 9-Kbit RAM blocks.

2 Bidirectional I/O pins that can be used as inputs or outputs; does not include dedicated clock input pins.

Cyclone FPGA series maximum user I/O

Device	Package/package size (mm)												
	T100 16 x 16	E/T1443 22 x 22	Q208 30 x 30	Q240 35 x 35	F256 17 x 17	U256 14 x 14	F324 19 x 19	F400 21 x 21	F484 23 x2 3	U484 19 x 19	F672 27 x 27	F780 29 x 29	F896 31 x 31
EP1C3	65	104											
EP1C4							249	301					
EP2C5		89	142		158								
EP3C5		94			182	182							
EP1C6		98		185	185								
EP2C8/A		85	138		182								
EP3C10		94			182	182							
EP1C12				173	185		249						
EP2C15A					152				315				
EP3C16		84		160	168	168			346	346			
EP1C20							233	301					
EP2C20/A				142	152				315				
EP3C25		82		148	156	156	215						
EP2C35									322	322	475		
EP3C40				128			195		331	331		535	
EP2C50									294	294	450		
EP3C55									327	327		377	
EP2C70											422		622
EP3C80									295	295		429	
EP3C120									283			531	

Cyclone FPGA series features

		Cyclone III family (1.2 V)							
		EP3C5	EP3C10	EP3C16	EP3C25	EP3C40	EP3C55	EP3C80	EP3C120
Density and speed	LEs	5,136	10,320	15,408	24,624	39,600	55,856	81,264	119,088
	Total RAM (Kbits)[1]	414	414	504	594	1,134	2,340	2,745	3,888
	M9K block (8 Kbits + 512 parity bits)[1]	46	46	56	66	126	260	305	432
	Speed grades (fastest to slowest)[2]	6, 7, 8	6, 7, 8	6, 7, 8	6, 7, 8	6, 7, 8	6, 7, 8	6, 7, 8	7, 8
Architectural features	Embedded processor	Nios II							
	18-bit x 18-bit/9-bit x 9-bit embedded multipliers	23/46	23/46	56/112	66/132	126/252	156/312	244/488	288/576
	True dual-port RAM	✓	✓	✓	✓	✓	✓	✓	✓
	Global clock networks	10	10	20	20	20	20	20	20
	PLLs/unique outputs	2/10	2/10	4/20	4/20	4/20	4/20	4/20	4/20
	Configuration file size (Mbits)	2.8	2.8	3.9	5.5	9.1	14.2	19	27.2
I/O features	I/O voltage levels supported	1.5, 1.8, 2.5, 3.0, 3.3							
	I/O standards supported	LVDS, RSDS, Mini-LVDS, LVPECL, Differential SSTL-18 (I and II), Differential SSTL-2 (I and II), 1.5 V Differential HSTL (I and II), 1.8V Differential HSTL (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.5V HSTL (I and II), PCI, PCI-X, PCI Express[3], LVTTL, LVCMOS, and PPDS							
	LVDS maximum data rate (Mbps) (receive/transmit)	875/840							
	LVDS channels	66	66	136	79	223	159	177	229
	RSDS maximum data rate (Mbps) (transmit)	360							
	Mini-LVDS maximum data rate (Mbps) (transmit)	400							
	Series on-chip termination	✓	✓	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓	✓	✓
External memory interfaces	Memory device supported	QDR II, DDR2, DDR, SDR							
	MegaCore controller with clear text datapath	✓							
	System timing and analysis	✓							
	Board layout guideline	✓							

[1] Kbits = 1,024 bits

[2] Not all packages are supported in all speed grades

[3] Requires external PHY device

Cyclone FPGA series features (continued)

		Cyclone II family (1.2 V)							Cyclone family (1.5 V)				
		EP2C5	EP2C8/A	EP2C15A	EP2C20/A	EP2C35	EP2C50	EP2C70	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Density and speed	LEs	4,608	8,256	14,448	18,752	33,216	50,528	68,416	2,910	4,000	5,980	12,060	20,060
	Total RAM (Kbits)[1]	117	162	234	234	472.5	580.5	1,125	58.5	76.5	90	234	288
	M4K RAM blocks (4 Kbits[1] + 512 parity bits)	26	36	52	52	105	129	250	13	17	20	52	64
	Speed grades (fastest to slowest)	-6, -7, -8							-6, -7, -8				
Architectural features	Embedded processor available	Nios II							Nios II				
	18-bit x 18-bit/9-bit x 9-bit embedded multipliers	13/26	18/36	26/52	26/52	35/70	86/172	150/300	–	–	–	–	–
	True dual-port RAM	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Global and regional clock networks	8	8	16	16	16	16	16	8	8	8	8	8
	PLLs/unique outputs	2/6	2/6	4/12	4/12	4/12	4/12	4/12	1/3	2/6	2/6	2/6	2/6
	Configuration file size (Mbits)	1.26	1.98	3.89	3.89	6.85	9.96	14.31	0.63	0.93	1.17	2.32	3.56
I/O features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3							1.5, 1.8, 2.5, 3.3				
	I/O standards supported	LVDS, RSDS, Mini-LVDS, LVPECL, Differential SSTL-18 (I and II), Differential SSTL-2 (I and II), 1.5V Differential HSTL (I and II), 1.8V Differential HSTL (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.5V HSTL (I and II), PCI, PCI-X, PCI Express[2], LVTTL, LVCMOS							LVDS, RSDS, Differential SSTL-2, SSTL-2 (I and II), SSTL-3 (I and II), PCI, LVTTL, LVCMOS				
	LVDS maximum data rate (Mbps) (receive/transmit)	805/640	805/640	805/640	805/640	805/640	805/640	805/640	640/640	640/640	640/640	640/640	640/640
	LVDS channels	60	79	136	136	209	197	265	34	129	72	103	129
	RSDS maximum data rate (Mbps) (transmit)	311	311	311	311	311	311	311	311	311	311	311	311
	Mini-LVDS maximum data rate (Mbps) (transmit)	311	311	311	311	311	311	311	–	–	–	–	–
	Series on-chip termination	✓	✓	✓	✓	✓	✓	✓	–	–	–	–	–
	Programmable drive strength	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
External memory interfaces	Memory devices supported	QDR II, DDR2, DDR, SDR							DDR, SDR				
	MegaCore controller with clear text datapath	✓							✓				
	System timing analysis	✓							✓				
	Board layout guidelines	✓							✓				

[1] Kbits = 1,024 bits

[2] Requires external PHY device

FOR MORE INFORMATION

Cyclone III FPGAs	www.altera.com/cyclone3
Cyclone II FPGAs	www.altera.com/cyclone2
Cyclone FPGAs	www.altera.com/cyclone
Training	www.altera.com/training

Arria GX low-cost FPGA family

90-nm FPGAs for PCI Express, Gigabit Ethernet, and Serial RapidIO up to 2.5 Gbps

With our new Arria™ GX FPGA family, you can quickly and easily connect custom logic to next generation devices offering PCI Express (x1 and x4), Gigabit Ethernet, and Serial RapidIO™ at speeds of up to 2.5 Gbps. If you have applications requiring bridging of either legacy parallel modules or devices to newer processors, you can take advantage of the device's proven transceiver technology. This device can also be used to complement those newer processors with custom designed blocks of logic.

Built on a foundation based on years of transceiver expertise and experience at Altera, Arria GX offers a physical coding sublayer (PCS) and physical medium attachment (PMA) interface that are cost-optimized versions of those in Stratix II GX.

Designing with the Arria GX family will present you with an easy way to interface custom logic to mainstream protocols at a very low total cost of ownership. You'll also benefit from an extensive set of reliable tools and a comprehensive support infrastructure.

Arria GX family features summary

Complete solution	Fully tested IP is available for PCI Express (x1 and x4), Gigabit Ethernet, and Serial RapidIO up to 2.5 Gbps. A simple and inexpensive development kit with reference designs is also available to demonstrate the simplicity of designing transceiver interfaces with Arria GX.
Best-in-class signal integrity	The Arria GX transceiver is based on the proven Stratix II GX transceiver and built with flip-chip packages. For those protocols supported by Arria GX, you'll get signal integrity that's close to what can be achieved by Stratix II GX.
Unparalleled software tools	The award-winning Quartus II Web Edition, as well as the subscription version, support all members of the Arria GX family. This makes designing with this family easy and inexpensive.
Extensive support network	Altera's team of several hundred field applications engineers (FAE) worldwide are available to help drive your success. This team is also backed by a global team of applications engineers in several Regional Service Centers around the world.

Arria GX FPGA family package and I/O matrix

36 Number indicates available user I/O pins.

Vertical migration (Same V_{CC}, GND, ISP, and input pins).

All Arria GX devices are offered in commercial and industrial temperatures and lead-free packages.

		Arria GX FPGAs (1.2 V) Low-cost, risk-free				
		EP1AGX20	EP1AGX35	EP1AGX50	EP1AGX60	EP1AGX90
FineLine BGA (F)	**484-pin (FlipChip)**	235	235	229	229	
	672-pin (Wirebond)					
	672-pin (FlipChip)					
	780-pin	341	341	350	350	
	896-pin					
	1,020-pin					
	1,152-pin			514	514	538
	1,508-pin					

Arria GX FPGA family features

		Arria GX FPGAs (1.2 V) Low-cost, risk-free				
		EP1AGX20	EP1AGX35	EP1AGX50	EP1AGX60	EP1AGX90
Density and speed	Equivalent LEs	21,580	33,520	50,160	60,100	90,220
	Adaptive logic modules (ALMs)	8,632	13,408	20,064	24,040	36,088
	Adaptive look-up tables (ALUTs)	17,264	26,816	40,128	48,080	72,176
	Total RAM (Kbits)[1]	1,229,184	1,348,416	2,475,072	2,528,640	4,477,824
	M512 RAM blocks (512 bits + 64 parity bits)	166	197	313	326	478
	M4K RAM blocks (4 Kbits[1] + 512 parity bits)	118	140	242	252	400
	M-RAM blocks (512 Kbits[1] + 65,536 parity bits)	1	1	2	2	4
	18-bit x 18-bit/9-bit x 9-bit embedded multipliers	40/80	56/112	104/208	128/256	176/352
	Speed grades (fastest to slowest)	-6	-6	-6	-6	-6
Architectural features	Embedded processor available	Nios II				
	DSP blocks	10	14	26	32	44
	I/O registers per I/O element	6	6	6	6	6
	True dual-port RAM	✓	✓	✓	✓	✓
	Global and regional clock networks	48	48	48	48	48
	PLLs/unique outputs	4	4	4 or 8	4 or 8	8
	Design security	–	–	–	–	–
	HardCopy® II device support	–	–	–	–	–
I/O features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3				
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS				
	True-LVDS maximum data rate (Mbps)	125–840				
	True-LVDS channels (receive/transmit)	31/29	31/29	42/42	42/42	47/45
	Embedded DPA circuitry	✓	✓	✓	✓	✓
	Series and differential on-chip termination	✓	✓	✓	✓	✓
	Programmable drive strength	–	–	–	–	–
	Transceiver (SERDES) data rate range	1.25 & 2.5 Gbps				
	Transceiver (SERDES) channels	4	4 or 8	4 or 8	4, 8 or 12	12
External memory interfaces	Memory devices supported	DDR2, DDR, SDR				
Configuration file sizes	Configuration file size (Mbits)	10	10	17	17	28

[1] Kbits = 1,024 bits

Stratix high-end FPGA series

The Stratix® FPGA series enables you to deliver high-performance, state-of-the-art products to market faster with lower risk and higher productivity. By combining high density, high performance, and a rich feature set, the Stratix FPGA series allows you to integrate more functions and maximize system performance. Using the Quartus II design software suite, along with a broad portfolio of IP, you can gain the highest level of productivity for large and complex team-based designs. Also contributing to the total solution are HardCopy® structured ASICs, which provide a seamless migration path to low-cost volume production. Backed by Altera's track record as a reliable and high-quality supplier, the Stratix FPGA series provides the tools you need to design with confidence.

Key features

- Industry's biggest and fastest FPGAs
- Lowest power high-end FPGAs
- Flexible and high-performance I/O pins
- Transceivers supporting speeds up to 6.375 Gbps
- Highest DSP and memory capabilities
- Path to low-cost HardCopy structured ASICs
- Volatile and non-volatile design security
- Quartus II design software for highest performance and productivity

65-nm high-performance, high-end FPGAs

Altera's Stratix III FPGAs were designed to address your design and business challenges, anticipate the unforeseen, and help you win in your market. The Stratix III family supports your applications' increased levels of integration and complexity with higher densities and performance, while decreasing power consumption. Its flexible and efficient logic architecture, enhanced memory blocks, and high-capacity DSP blocks meet your system's most demanding requirements.

Specifically designed for ease of use and rapid system integration, the Stratix III FPGA family offers three variants optimized to meet different application needs. Stratix III L FPGAs deliver balanced logic, memory, and DSP resources for general-purpose applications; Stratix III E FPGAs provide enhanced memory and DSP resources for memory- and DSP-intensive applications; Stratix III GX FPGAs offer integrated transceivers for high-bandwidth interface applications. All three variants include fast, flexible, and robust I/O connectivity for greater system performance.

Stratix III family features summary

Programmable Power Technology	The core logic, routing, memory, and DSP blocks in Stratix III FPGAs have fine-grained control over whether a specific tile is in high-speed mode or low-power mode. Quartus II design software automatically applies the high-speed mode to all parts of the design that require the highest performance, utilizing the low-power mode for all other parts of the FPGA. Leakage power is reduced by about 70 percent for the portions of the design implemented with low-power mode.
Selectable core voltage	The core voltage of Stratix III FPGAs can be set depending on performance requirements—to the 1.1-V setting for the highest performance and 0.9V for the lowest power. The 0.9-V setting reduces dynamic power by 55 percent over previous generation 1.2-V devices. The core voltage setting is independent of Programmable Power Technology.
ALMs	ALMs provide industry-leading performance and logic density with a patented fracturable eight-input LUT, two dedicated adders, and two registers. ALMs deliver 80 percent greater logic density than competitive architectures along with more registers, resulting in increased performance through reduced total logic levels and associated routing.
MultiTrack interconnect	Connections between ALMs, TriMatrix memory blocks, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive technology. Compared to competitors, the MultiTrack interconnect offers nearly three times the number of one-hop interconnects between logic array blocks (LABs), maximizing performance for challenging, time-critical logic. The interconnect has the industry's largest single hop span of five LABs, minimizing routing congestion and further improving performance and routability. The Quartus II compiler automatically places critical design paths on faster interconnects to maximize performance.

Stratix III family features summary (continued)

TriMatrix memory	TriMatrix memory offers 3 memory block sizes to suit complex design needs: 640-bit MLAB blocks, 9-Kbit M9K blocks, and 144-Kbit M144K blocks. With up to 21 Mbits of memory performing at over 600 MHz and features such as dual-port RAM and integrated error correction code (ECC), TriMatrix memory is more flexible and efficient, and provides higher memory bandwidth than any other memory architecture.
DSP blocks	DSP blocks provide twice as many multiplier resources as competing architectures, with up to 896 18-bit x 18-bit multipliers on the EP2SE110 device. DSP blocks include all associated pipelining, adders, and accumulators. They are configurable to support 9-bit x 9-bit, 12-bit x 12-bit, 18-bit x 18-bit, or 36-bit x 36-bit multipliers at up to 550 MHz.
External memory interface circuitry	Stratix III FPGAs provide the industry's highest performance external DRAM and SRAM memory interfaces, including DDR3, PVT compensated dedicated hard I/O structures with on-chip termination, trace compensation, read/write leveling, and half- and full-rate registered outputs. Complete solutions, including easy-to-use IP, hardware development platforms, and comprehensive timing analysis, are available to minimize risk and speed time to market.
High-speed single-ended I/O support	Up to 24 modular I/O banks with dedicated DQ/DQS circuitry, programmable slew rate, programmable drive strength, programmable output delay, on-chip termination, and dynamic trace compensation maximize I/O flexibility and performance for over 40 industry standards to optimally match your system requirements.
High-speed differential I/O support	Optimized LVDS I/O pins provide high performance and excellent signal integrity with half the capacitance of competitive devices. Stratix III LVDS supports hard DPA and serializer/deserializer (SERDES) blocks with clock forwarding for clock data recovery in high-speed chip-to-chip applications. Wizards make differential I/O configuration straightforward and easy.
Dynamic phase alignment (DPA)	DPA minimizes bit errors and simplifies PCB layout and timing management for high-speed data transfer. DPA eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems.
On-chip termination	Serial, parallel, dynamic, and differential on-chip termination simplifies design and reduces component count. Dynamic on-chip termination enables support for next-generation memory interface designs that must dynamically switch between serial and parallel termination. Digital calibration circuitry provides industry-leading on-chip termination tolerance within 10 percent.
Clock management features	Each product family has up to 12 PLLs with up to 10 unique customizable outputs per PLL ranging from 5 to 720 MHz. There are also up to 16 global, 88 quadrant, and 208 periphery clocks. Advanced clock management features include PLL reconfiguration, frequency synthesis, programmable phase shift, programmable delay shift, external feedback, and programmable bandwidth for all on- and off-chip clocking requirements.
Design security	To prevent IP theft and product tampering, the devices feature configuration bitstream encryption using the advanced encryption standard (AES) and 256-bit key. Stratix III FPGAs are the industry's only design security solution with both non-volatile and volatile key options. The non-volatile key is more practical, easy to use and low cost, while the volatile key is reprogrammable.
Remote system upgrades	This capability enables reliable and safe deployment of in-system enhancements and bug fixes.
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support ensures proper device operation independent of the power-up sequence.
Automatic SEU detection circuitry	The devices feature automatic SEU detection circuitry utilizing 32-bit CRC with criticality processor to determine the importance of error.
Nios II embedded processor support	Nios II embedded processors reduce cost, increase flexibility, and offer an ideal replacement for low-cost discrete microprocessors. Nios II soft processor support for Stratix III FPGAs offers over 250-DMIPS performance.
HardCopy structured ASIC series support	This pin-compatible structured ASIC reduces cost and power for volume applications.

Stratix II

90-nm high-performance, high-density FPGAs

Stratix II devices are the industry's leading 90-nm high-density, high-performance FPGAs. Built on an ALM logic structure to maximize performance and minimize power, Stratix II devices on average deliver 50 percent faster performance than prior-generation FPGAs. Stratix II devices set the standard for the next generation of logic architectures. Stratix II FPGAs include a risk-free path to HardCopy II structured ASICs, which can further increase performance, reduce power, and minimize costs.

Stratix II family features summary

ALMs	ALMs provide industry-leading performance and logic density with a patented fracturable eight-input LUT, two dedicated adders, and two registers. ALMs deliver 80 percent greater logic density than competitive architectures along with more registers, resulting in increased performance through reduced total logic levels and associated routing.
MultiTrack interconnect	Connections between ALMs, TriMatrix memory blocks, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive technology. Compared to competitors, the MultiTrack interconnect offers nearly three times the number of one-hop interconnects between LABs, maximizing performance for challenging, time-critical logic. The interconnect has the industry's largest single hop span of five LABs, minimizing routing congestion and further improving performance and routability. The Quartus II compiler automatically places critical design paths on faster interconnects to maximize performance.
TriMatrix memory	TriMatrix memory in Stratix II FPGAs provides up to 9 Mbits of memory in three block sizes: 512 bits in the M512, 4 Kbits in the M4K, and 500 Kbits in the M-RAM blocks. TriMatrix memory includes parity checking and is capable of up to 550-MHz performance.
DSP blocks	Each DSP block includes multipliers with associated pipelining, adders, and accumulators. Stratix II FPGAs include up to 96 DSP blocks offering 384 18-bit x 18-bit multipliers that operate at up to 450 MHz. Each multiplier can be configured as 9-bit x 9-bit, 18-bit x 18-bit, or 36-bit x 36-bit multipliers.
External memory interface circuitry	Fully characterized and hardware-validated circuitry provides flexible, high-performance interfaces to the latest external DRAM and SRAM memory technologies. Complete solutions, including easy-to-use IP, hardware development platforms, and comprehensive timing analysis, are available to minimize risk and speed time to market.
High-speed differential I/O support	Optimized LVDS I/O with DPA and SERDES capability provides high performance and excellent signal integrity. Wizards make differential I/O configuration straightforward and easy.
DPA	DPA maximizes signal integrity and simplifies PCB layout and timing management for high-speed data transfer. DPA eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems.
On-chip termination	Serial and differential on-chip termination simplifies design and reduces component count. Digital calibration circuitry provides industry-leading on-chip termination tolerance within five percent.
Clock management features	Up to 12 PLLs and up to 48 system clocks. Advanced clock management features include PLL reconfiguration, spread-spectrum clocking, frequency synthesis, programmable phase shift, programmable delay shift, external feedback, and programmable bandwidth for all on- and off-chip clocking requirements.
Design security	Configuration bitstream encryption using 128-bit AES; prevents IP theft and product tampering. The non-volatile key storage makes the solution reliable, easy to use, and low cost.
Remote system upgrades	Enables reliable and safe deployment of in-system enhancements and bug fixes.
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support ensures proper device operation independent of the power-up sequence.
Automatic SEU detection circuitry	Features automatic SEU detection circuitry utilizing 32-bit CRC.
Nios II embedded processor support	Nios II embedded processors reduce cost, increase flexibility, and offer an ideal replacement for low-cost discrete microprocessors. Nios II soft processor support for Stratix II FPGAs offers over 200-DMIPS performance.
HardCopy II structured ASIC support	Reduce cost and power for volume applications using this pin-compatible structured ASIC.

90-nm high-performance, high-density FPGAs with 6.375-Gbps transceivers

Altera's Stratix II GX devices deliver all the benefits of Stratix II devices plus up to 20 low-power, high-speed transceiver channels. The transceivers support all data rates spanning from 600 Mbps to 6.375 Gbps. They have dynamically configurable transmit pre-emphasis and receiver equalization to optimize signal integrity under adverse channel conditions. The transceivers are capable of driving FR-4 backplanes at 6.375 Gbps and have proven to be interoperable with backplanes and transceivers from multiple vendors.

In addition, the PCS hard IP, which is part of the transceiver block, saves valuable logic resources and simplifies protocol support. Stratix II GX devices incorporate protocol-specific PCS blocks for the following protocols: PCI Express, Common Electrical Interface 6.375 Gbps (CEI-6G), serial digital interface (SDI), XAUI, SONET, Gigabit Ethernet, Serial RapidIO, and SerialLite II. Stratix II GX devices also have 8b/10b encoder/decoders that are bypassable for proprietary protocols.

The Stratix II GX family is part of a complete serial protocol solution that includes IP cores, development boards, reference designs, and evaluation tools to ensure successful protocol compliance and optimal signal integrity.

Stratix II GX family features summary

Excellent signal integrity, 600 Mbps - 6.375 Gbps	The transmitter has low jitter generation and up to 500 percent pre-emphasis. The receiver has excellent jitter tolerance and up to 17-dB of equalization.
Low power	The transceiver dissipates 200 mW per channel at 6.375 Gbps and only 140 mW per channel at 3.125 Gbps.
PCS support (hard IP)	The transceiver supports the following PCS blocks: PCI Express, PIPE-Compliant PCS, CEI-6G, 8b/10b encoder/decoder, XAUI state machine and channel bonding, Gigabit Ethernet state machine, SONET, and 8/10/16/20/32/40-bit interface (to logic).
System-level diagnostics	Serial loopback, reverse serial loopback, psuedo-random binary sequence (PRBS) generator checker, and register-based interface facilitate dynamic reconfiguration of pre-emphasis, equalization, and differential output voltage.

130-nm high-performance, high-density FPGAs

The density of Stratix devices ranges from 10,570 to 79,040 LEs, with up to 7 Mbits of embedded RAM and 88 18-bit x 18-bit multipliers. Stratix devices have up to 12 PLLs, 40 system clocks, and support for many single-ended and differential I/O electrical standards. Stratix FPGAs are based on a 1.5-V, 130-nm, all-layer-copper SRAM process.

Stratix family features summary

MultiTrack interconnect	Connections between LEs, TriMatrix memory blocks, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive technology. Compared to competitors, the MultiTrack interconnect offers nearly three times the number of one-hop interconnects between LABs, maximizing performance for challenging, time-critical logic. The interconnect has the industry's largest single hop span of five LABs, minimizing routing congestion and further improving performance and routability. The Quartus II compiler automatically places critical design paths on faster interconnects to maximize performance.
TriMatrix memory	TriMatrix memory in Stratix FPGAs provides up to 7 Mbits of memory in three block sizes: 512 bits in the M512, 4 Kbits in the M4K, and 500 Kbits in the M-RAM blocks. TriMatrix memory includes parity checking and is capable of up to 320-MHz performance.
DSP blocks	Each DSP block includes four 18-bit x 18-bit multipliers with associated pipelining, adders, and accumulators. Configurations can support any bit-width up to 36 bits x 36 bits. Stratix FPGAs include up to 22 DSP blocks offering 88 18-bit x 18-bit multipliers that operate at up to 275 MHz.
High-speed differential I/O support	Optimized LVDS I/O pins provide high performance and excellent signal integrity. Wizards make differential I/O configuration straightforward and easy.
On-chip termination	Serial and differential on-chip termination simplifies design and reduces component count. Digital calibration circuitry provides industry-leading on-chip termination tolerance.
Clock management features	Up to 12 PLLs and up to 48 system clocks. Advanced clock management features include PLL reconfiguration, spread-spectrum clocking, frequency synthesis, programmable phase shift, programmable delay shift, external feedback, and programmable bandwidth for all on- and off-chip clocking requirements.
Remote system upgrades	Enable reliable, safe deployment of in-system upgrades and bug fixes.
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support that ensures proper device operation independent of the power-up sequence.
Automatic SEU detection circuitry	Features automatic SEU detection circuitry utilizing 32-bit CRC.
Nios II embedded processor support	Nios II embedded processors reduce cost, increase flexibility, and offer an ideal replacement for low-cost discrete microprocessors. Nios II soft processor support for Stratix FPGAs offers over 150-DMIPS performance.
HardCopy structured ASIC support	Reduce cost for volume applications using this pin-compatible structured ASIC.

Stratix GX

130-nm high-performance, high-density FPGAs with 3.1875-Gbps transceivers

Stratix GX FPGAs combine Altera's second-generation transceivers with the award-winning Stratix FPGA architecture. Stratix GX FPGAs have up to 20 transceivers operating from 500 Mbps to 3.1875 Gbps, which can easily drive 40-inch backplanes. Stratix GX devices, with their excellent transmit pre-emphasis, receiver equalization, and 8b/10b encoder/decoder circuitry, deliver a robust transceiver solution.

Stratix GX devices also incorporate dedicated SERDES and DPA circuitry into 45 source-synchronous differential I/O pins, enabling the devices to operate at up to 1 Gbps. DPA automatically compensates for clock-to-channel skew on a channel-per-channel basis, thereby simplifying board layout and design. For new designs, Stratix II GX devices provide better performance and cost attributes than Stratix GX devices.

Stratix GX family features summary

500-Mbps - 3.1875-Gbps transceiver blocks	Embedded transceiver blocks, including 8b/10b encoder/decoder circuitry, provide support for high-speed applications, such as: SerialLite II, XAUI, Gigabit Ethernet, 1G, 2G, and 10G Fibre Channel, Serial RapidIO, SONET/SDH (synchronous digital hierarchy), PCI Express, Open Base Station Architecture Initiative (OBSAI), and serial digital interface (SDI).
Excellent drive strength capability	Transceiver capabilities, embedded programmable transmit pre-emphasis, and embedded receiver equalization combine to enable signal drive capability across a 40-inch FR4 backplane and two backplane connectors.
Low power consumption	450-mW power consumption per 4-channel transceiver block simplifies board design.
Source-synchronous differential I/O signaling with DPA	Support for high-speed I/O standards and high-speed interfaces such as 10 Gigabit Ethernet XSBI, SFI-4, SPI-4 Phase 2 (packet over SONET (POS)-PHY Level 4), HyperTransport technology, and parallel RapidIO standards, at up to 1 Gbps to complement transceiver bandwidth.
DPA	Maximizes signal integrity and simplifies PCB layout and timing management for high-speed data transfer. Eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems.
High-performance Stratix architecture	Highly optimized FPGA architecture provides innovative routing for block-based design and maximum system performance. Features such as TriMatrix memory, DSP blocks, and clock management circuitry enable full system implementation.

Stratix FPGA series package and I/O matrices

342 Number indicates available user I/O pins.

Vertical migration (Same V_{CC}, GND, ISP, and input pins).

All Stratix series devices are offered in commercial and industrial temperatures and lead-free packages.

		Stratix III L FPGAs Balanced logic, memory, and DSP						Stratix III E FPGAs Memory/DSP enhanced			
		EP3SL50	EP3SL70	EP3SL110	EP3SL150	EP3SL200	EP3SL340	EP3SE50	EP3SE80	EP3SE110	EP3SE260[1]
FBGA (F)	**484-pin (FlipChip)**	288	288					288			
	780-pin	480	480	480	480			480	480	480	
	1,152-pin			736	736	736			736	736	736
	1,517-pin					864	960				960
	1,760-pin						1,104				

[1] EP3SE260 FPGAs are the optimum solution for both logic (Stratix III L) and DSP/memory (Stratix III E) applications at this density.

Stratix FPGA series package and I/O matrices (continued)

342 Number indicates available user I/O pins.

Vertical migration (Same V_{CC}, GND, ISP, and input pins). User I/O may be less than labelled for vertical migration.

All Stratix series devices are offered in commercial and industrial temperatures and lead-free packages.

		Stratix II FPGAs (1.2 V) High density, high performance						Stratix II GX FPGAs (1.2 V) 6.375-Gbps transceivers							
		EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180	EP2SGX30C	EP2SGX30D	EP2SGX60C	EP2SGX60D	EP2SGX60E	EP2SGX90E	EP2SGX90F	EP2SGX130G
FBGA (F)	**484-pin (FlipChip)**	342	342	334											
	672-pin (FlipChip)	366	500	492											
	780-pin				534	534		361	361	364	364				
	1,020-pin			718	758	742	742								
	1,152-pin											534	558		
	1,508-pin				902	1,126	1,170							650	734
Hybrid FBGA (H)	**484-pin**				308										

345 Number indicates available user I/O pins.

Vertical migration (Same V_{CC}, GND, ISP, and input pins). User I/O may be less than labelled for vertical migration.

All Stratix series devices are offered in commercial and industrial temperatures and lead-free packages.

		Stratix FPGAs (1.5 V) High density, high performance							Stratix GX FPGAs (1.5 V) 3.1875-Gbps transceivers						
		EP1S10	EP1S20	EP1S25	EP1S30	EP1S40	EP1S60	EP1S80	EP1SGX10C	EP1SGX10D	EP1SGX25C	EP1SGX25D	EP1SGX25F	EP1SGX40D	EP1SGX40G
FBGA (F)	**672-pin (FlipChip)**								362	362	455	455			
	672-pin (wire bond)	345	426	473											
	780-pin	426	586	697	589	615									
	1,020-pin			706	726	773	773	773				607	607	624	624
	1,152-pin														
	1,508-pin					822	1,022	1,203							
Ball-Grid Array (B)	**672-pin**	356	426	473											
	956-pin				683	683	683	683							

Stratix FPGA series features

		Stratix III L FPGAs Balanced logic, memory, and DSP						Stratix III E FPGAs Memory/DSP enhanced			
		EP3SL50	EP3SL70	EP3SL110	EP3SL150	EP3SL200	EP3SL340	EP3SE50	EP3SE80	EP3SE110	EP3SE260[1]
Density and speed	Equivalent LEs	47,500	67,500	106,500	142,000	198,900	338,000	47,500	80,000	106,500	254,400
	ALMs	19,000	27,000	42,600	56,800	79,560	135,200	19,000	32,000	42,600	101,760
	Registers[2]	38,000	54,000	85,200	113,600	159,120	270,400	38,000	64,000	85,200	203,520
	M9K memory blocks	108	150	275	355	468	1,040	400	495	639	864
	M144K memory blocks	6	6	12	16	24	48	12	12	16	48
	Embedded memory (Kbits)	1,836	2,214	4,203	5,499	7,668	16,272	5,328	6,183	8,055	14,688
	MLAB memory (Kbits)	594	844	1,344	1,781	2,500	4,219	594	1,000	1,344	3,188
	Max 18-bit x 18-bit multipliers	216	288	288	384	576	576	384	672	896	768
	Speed grades (fastest to slowest)	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4
Architectural features	Embedded processor available	Nios II									
	Global clock networks	16	16	16	16	16	16	16	16	16	16
	Regional clock networks	48	48	48	48	88	88	48	48	48	88
	Periphery clock networks	104	104	208	208	208	208	104	208	208	208
	PLLs/unique outputs	4/34	4/34	8/68	8/68	12/96	12/96	8/68	12/96	12/96	12/96
	Design security	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	HardCopy series device support[3]	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0									
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS									
	True-LVDS maximum data rate (Mbps)	125 - 1,250									
	Number of LVDS channels (receive/transmit)	56/56	56/56	88/88	88/88	112/112	132/132	56/56	88/88	88/88	112/112
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Series and differential on-chip termination	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
External memory interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR									
Configuration file sizes	Configuration file size (Mbits)[3]	22	22	47	47	66	120	26	48	48	93

[1] EP3SE260 FPGAs are the optimum solution for both logic (Stratix III L) and DSP/memory (Stratix III E) applications at this logic density.

[2] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which can increase total register count by an additional 50 percent.

[3] This data is preliminary.

Stratix FPGA series features (continued)

		Stratix II FPGAs (1.2 V) High density, high performance					
		EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180
Density and speed	Equivalent LEs	15,600	33,880	60,440	90,960	132,540	179,400
	ALMs	6,240	13,552	24,176	36,384	53,016	71,760
	Adaptive look-up tables (ALUTs)	12,480	27,104	48,352	72,768	106,032	143,520
	Total RAM (Kbits)[1]	410	1,338	2,485	4,415	6,590	9,163
	M512 RAM blocks (512 bits + 64 parity bits)	104	202	329	488	699	930
	M4K RAM blocks (4 Kbits[1] + 512 parity bits)	78	144	255	408	609	768
	M-RAM blocks (512 Kbits[1] + 65,536 parity bits)	0	1	2	4	6	9
	18-bit x 18-bit/9-bit x 9-bit embedded multipliers	48/96	64/128	144/288	192/384	252/504	384/768
	Speed grades (fastest to slowest)	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5
Architectural features	Embedded processor available	Nios II					
	DSP blocks	12	16	36	48	63	96
	I/O registers per I/O element	6	6	6	6	6	6
	True dual-port RAM	✓	✓	✓	✓	✓	✓
	Global and regional clock networks	48	48	48	48	48	48
	PLLs/unique outputs	6/28	6/28	12/56	12/56	12/56	12/56
	Design security	✓	✓	✓	✓	✓	✓
	HardCopy II device support	–	✓	✓	✓	✓	✓
I/O features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3					
	I/O standards supported	LVDS, LVPECL, HyperTransport™, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II),1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS					
	True-LVDS maximum data rate (Mbps)	125 - 1,000					
	True-LVDS channels (receive/transmit)	38/38	58/58	80/84	114/118	152/156	152/156
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓
	Series and differential on-chip termination	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓
External memory interfaces	Memory devices supported	DDR2, DDR, QDR II, RLDRAM II, SDR					
Configuration file sizes	Configuration file size (Mbits)	5	10	17	28	40	53

[1] Kbits = 1,024 bits

Stratix FPGA series features (continued)

		Stratix II GX FPGAs (1.2 V) 6.375-Gbps transceivers							
		EP2SGX30C	EP2SGX30D	EP2SGX60C	EP2SGX60D	EP2SGX60E	EP2SGX90E	EP2SGX90F	EP2SGX130G
Density and speed	Equivalent LEs	33,880	33,880	60,440	60,440	60,440	90,960	90,960	132,540
	ALMs	13,552	13,552	24,176	24,176	24,176	36,384	36,384	53,016
	ALUTs	27,104	27,104	48,352	48,352	48,352	72,768	72,768	106,032
	Total RAM (Kbits)[1]	1,338	1,338	2,485	2,485	2,485	4,415	4,415	6,590
	M512 RAM blocks (512 bits + 64 parity bits)	202	202	329	329	329	488	488	699
	M4K RAM blocks (4 Kbits[1] + 512 parity bits)	144	144	255	255	255	408	408	609
	M-RAM blocks (512 Kbits[1] + 65,536 parity bits)	1	1	2	2	2	4	4	6
	18-bit x 18-bit/9-bit x 9-bit embedded multipliers	64/128	64/128	144/288	144/288	144/288	192/384	192/384	252/504
	Speed grades (fastest to slowest)	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5
Architectural features	Embedded processor available	Nios II							
	DSP blocks	16	16	36	36	36	48	48	63
	I/O registers per I/O element	6	6	6	6	6	6	6	6
	True dual-port RAM	✓	✓	✓	✓	✓	✓	✓	✓
	Global and regional clock networks	48	48	48	48	48	48	48	48
	PLLs/unique outputs	4/18	4/18	4/18	4/18	8/36	8/36	8/36	8/36
	Design security	✓	✓	✓	✓	✓	✓	✓	✓
	HardCopy II device support	–	–	–	–	–	–	–	–
I/O features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3							
	I/O standards supported	LVDS, LVPECL, HyperTransport™, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS							
	True-LVDS maximum data rate (Mbps)	125 - 1,000							
	True-LVDS channels (receive/transmit)	31/29	31/29	31/29	31/29	42/42	47/45	59/59	73/71
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓	✓	✓
	Series and differential on-chip termination	✓	✓	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓	✓	✓
	Transceiver (SERDES) data rate range	600 Mbps - 6.375 Gbps							
	Transceiver (SERDES) channels	4	8	4	8	12	12	16	20
External memory interfaces	Memory devices supported	DDR2, DDR, QDR II, RLDRAM II, SDR							
Configuration file sizes	Configuration file size (Mbits)	10	10	17	17	17	28	28	40

[1] Kbits = 1,024 bits

Stratix FPGA series features (continued)

		Stratix FPGAs (1.5 V) High density, high performance						
		EP1S10	EP1S20	EP1S25	EP1S30	EP1S40	EP1S60	EP1S80
Density and speed	LEs	10,570	18,460	25,660	32,470	41,250	57,120	79,040
	Total RAM (Kbits)[1]	899	1,630	1,899	3,239	3,344	5,093	7,253
	M512 RAM blocks (512 bits + 64 parity bits)	94	194	224	295	384	574	767
	M4K RAM blocks (4 Kbits[1] + 512 parity bits)	60	82	138	171	183	292	364
	M-RAM blocks (512 Kbits[1] + 65,536 parity bits)	1	2	2	4	4	6	9
	18-bit x 18-bit/9-bit x 9-bit embedded multipliers	24/48	40/80	40/80	48/96	56/112	72/144	88/176
	Speed grades (fastest to slowest)	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7
Architectural features	Embedded processor available	Nios II						
	DSP blocks	6	10	10	12	14	18	22
	I/O registers per I/O element	6	6	6	6	6	6	6
	True dual-port RAM	3	3	3	3	3	3	3
	Global and regional clock networks	36	36	36	40	40	40	40
	PLLs/unique outputs	6/32	6/32	6/32	10/40	12/52	12/52	12/52
	Design security	–	–	✓	✓	✓	✓	✓
I/O features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3						
	I/O standards supported	LVDS, LVPECL, HyperTransport™, 3.3-V PCML, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), SSTL-3 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, Compact-PCI, PCI-X 1.0, AGP (1x and 2x), GTL, GTL+, CTT, LVTTL, LVCMOS						
	True-LVDS maximum data rate (Mbps)	840						
	True-LVDS channels (receive/transmit)	44/44	66/66	78/78	80/80	80/80	80/80	80/80
	Medium-speed LVDS channels	–	–	–	462	462	462	462
	Embedded DPA circuitry	–	–	–	–	–	–	–
	Series and differential on-chip termination	✓	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓	✓
External memory interfaces	Memory devices supported	QDR II, QDR, ZBT, DDR, SDR						
Configuration file sizes	Configuration file size (Mbits)	3.53	5.9	7.89	10.38	12.39	17.54	23.83

[1] Kbits = 1,024 bits

Stratix FPGA series features (continued)

		Stratix GX FPGAs (1.5 V) 3.1875-Gbps transceivers						
		EP1SGX10C	EP1SGX10D	EP1SGX25C	EP1SGX25D	EP1SGX25F	EP1SGX40D	EP1SGX40G
Density and speed	LEs	10,570	10,570	25,660	25,660	25,660	41,250	41,250
	Total RAM (Kbits)[1]	899	899	1,899	1,899	1,899	3,344	3,344
	M512 RAM blocks (512 bits + 64 parity bits)	94	94	224	224	224	384	384
	M4K RAM blocks (4 Kbits[1] + 512 parity bits)	60	60	138	138	138	183	183
	M-RAM blocks (512 Kbits[1] + 65,536 parity bits)	1	1	2	2	2	4	4
	18-bit x 18-bit/9-bit x 9-bit embedded multipliers	24/48	24/48	40/80	40/80	40/80	56/112	56/112
	Speed grades (fastest to slowest)	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7
Architectural features	Embedded processor available	Nios II						
	DSP blocks	6	6	10	10	10	14	14
	I/O registers per I/O element	6	6	6	6	6	6	6
	True dual-port RAM	3	3	3	3	3	3	3
	Global and regional clock networks	36	36	36	36	36	40	40
	PLLs/unique outputs	4/26	4/26	4/26	4/26	4/26	8/42	8/42
	HardCopy device support	–	–	–	–	–	–	–
I/O features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3						
	I/O standards supported	LVDS, LVPECL, HyperTransport™, 3.3-V PCML, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), SSTL-3 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, Compact-PCI, PCI-X 1.0, AGP (1x and 2x), GTL, GTL+, CTT, LVTTL, LVCMOS						
	True-LVDS maximum data rate (Mbps)	1,000						
	True-LVDS channels (receive/transmit)	22/22	22/22	39/39	39/39	39/39	45/45	45/45
	Medium-speed LVDS channels	–	–	–	–	–	–	–
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓	✓
	Series and differential on-chip termination	✓	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓	✓
	Transceiver (SERDES) data rate range	500 Mbps - 3.1875 Gbps						
	Transceiver (SERDES) channels	4	8	4	8	16	8	20
External memory interfaces	Memory devices supported	QDR II, QDR, ZBT, DDR, SDR						
Configuration file sizes	Configuration file size (Mbits)	3.58	3.58	7.95	7.95	7.95	12.53	12.53

[1] Kbits = 1,024 bits

FOR MORE INFORMATION

Stratix III FPGAs	www.altera.com/stratix3
Stratix II FPGAs	www.altera.com/stratix2
Stratix FPGAs	www.altera.com/stratix
Stratix II GX transceiver FPGAs	www.altera.com/stratix2gx
Stratix GX transceiver FPGAs	www.altera.com/stratixgx
Training	www.altera.com/training

HardCopy structured ASIC series

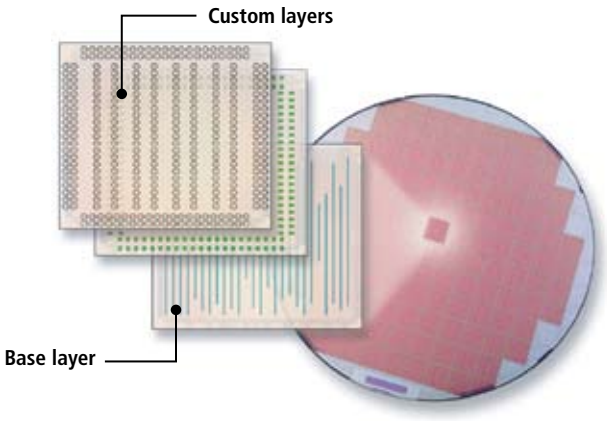
Need to move quickly from prototype to low-cost production? Altera's HardCopy structured ASIC series delivers unmatched product development flexibility and speed, enabling you to make the most of your engineering resources and budget. HardCopy structured ASICs are the market's only devices to offer a seamless prototype-to-production process for guaranteed success. Through its unique FPGA front-end design flow, the HardCopy series enables you to use Altera's Stratix series FPGAs to develop, verify, and finalize your system design before you commit to silicon.

Structured ASICs bridge the gap between standard cell ASIC technology and FPGAs, offering low unit costs combined with faster development times. Structured ASICs start with standard, pre-tested base layers of logic and hard IP. The proprietary design is then implemented on the top few metal layers. Within your existing design environment, utilize Stratix FPGAs as your design's front end and then test it in-system. When you're done, Altera's HardCopy Design Center seamlessly migrates your design to HardCopy structured ASICs in just 7 to 11 weeks.

Key features

- Ability to test designs in Stratix series FPGAs
- Seamless migration to structured ASIC when design is completed and volumes assured
- Dramatically lower power compared to FPGAs
- Turnkey migration from FPGA prototype to structured ASIC in Altera's HardCopy Design Center
- Ability to design with Quartus II software in conjunction with tools from Cadence, Mentor Graphics®, Synopsys, and Synplicity
- Lower embedded systems costs with Nios II processors

Structured ASIC



HardCopy® II

90-nm structured ASICs with guaranteed success

The 1.2-V, 90-nm HardCopy II family builds on the success of Altera's first two HardCopy families. HardCopy II devices offer 2.2 million ASIC gates for logic prototyping, 8.8 million bits of memory, and over 350-MHz system performance. Compared to FPGAs, HardCopy II devices offer over 50 percent core power reduction and higher core performance.

Use Stratix II FPGAs for prototyping and testing, and then migrate to HardCopy II devices — we'll guarantee success for high-volume production devices. HardCopy II devices replace the ALM-based logic in Stratix II FPGAs with a fine-grained array of HCells to deliver as low as one-tenth the cost of the Stratix II FPGA in which the design was verified. The HardCopy II family delivers seamless FPGA migration while providing the density, cost, performance, and power benefits of ASIC technology.

HardCopy II family features summary

Clock management	Up to 12 programmable PLLs, providing robust clock management and frequency synthesis capabilities for maximum system performance. The PLLs provide high-end features, including clock switchover, PLL reconfiguration, spread-spectrum clocking, frequency synthesis, programmable phase shift, programmable delay shift, external feedback, and programmable bandwidth.
Differential I/O support	Support for high-speed differential I/O for data rates up to 1 Gbps to address the high-performance needs of emerging I/O interfaces, including support for the LVDS, LVPECL, and HyperTransport™ standards.
External memory interfaces	Advanced external memory interface support, allowing you to integrate external high-density SRAM and DRAM devices into complex system designs without degrading data-access performance.
On-chip termination	Series and differential on-chip termination support can simplify board layout by minimizing the number of external resistors needed.
Single-ended I/O standards	High-bandwidth, single-ended I/O interface standards support (SSTL, HSTL, PCI, and PCI Express).
Source-synchronous protocols	Support for a wide array of high-speed interface standards, including SPI-4.2, SFI-4, 10 Gigabit Ethernet XSBI, and RapidIO.
TriMatrix memory	Up to 8.8 Mbits of RAM—configurable M4K and M-RAM embedded RAM blocks for a wide range of features.

HardCopy®

130-nm structured ASICs with guaranteed success

Altera's HardCopy Stratix family is manufactured on 1.5-V, 130-nm process technology. These devices use Stratix FPGAs for prototyping and have the same LE architecture as Stratix devices. With 300,000 to 1,000,000 ASIC gates and up to 5,600,000 bits of memory, HardCopy Stratix devices offer a 50 percent performance increase and 40 percent lower power consumption than the Stratix prototype.

HardCopy Stratix devices support a wide range of high-speed interfaces —including the SPI-4 Phase 2, 10-Gigabit Ethernet XSBI, and RapidIO interfaces. They also support the LVDS, LVPECL, and HyperTransport™ high-speed I/O standards. These advanced capabilities allow designers to connect high-speed memory devices like QDR and zero-bus turnaround (ZBT) SRAMs.

HardCopy Stratix family features summary

Clock management	Support for up to 12 programmable PLLs and 40 system clocks.
Differential I/O support	Up to 152 high-speed differential I/O channels with 80 channels optimized for data rates up to 840 Mbps, and support for emerging I/O interfaces including the LVDS, LVPECL, PCML, and HyperTransport standards.
DSP blocks	Up to 22 DSP blocks.
DSP performance	Up to 463 giga multiply-accumulate operations per second (GMACS) of DSP throughput.
Embedded test capability	Available.
External memory interfaces	External memory interface to high-density SRAM and DRAM devices.
High-speed interfaces	Support for a wide array of high-speed interface standards, such as the SPI-4 Phase 2, SFI-4, 10-Gigabit Ethernet XSBI, HyperTransport™, RapidIO, and UTOPIA IV standards.
On-chip termination	Support for differential on-chip termination.
Single-ended I/O support	Support for high-bandwidth single-ended I/O interface standards, such as SSTL, HSTL, GTL, GTL+, CTT, and PCI-X.
TriMatrix memory	Up to 5.6 Mbits of TriMatrix memory.

HardCopy structured ASIC series package and I/O matrix

951 Number indicates available user I/O pins.

All HardCopy series devices are offered in commercial and industrial temperatures and lead-free packages.

		HardCopy II (1.2 V) structured ASIC						HardCopy Stratix (1.5 V) structured ASIC				
		HC210W	HC210	HC220W	HC220	HC230	HC240	HC1S25	HC1S30	HC1S40	HC1S60	HC1S80
FBGA (F)	484-pin (wire bond)	308										
	484-pin (FlipChip)		334									
	672-pin (wire bond)			440				473				
	672-pin (FlipChip)				492							
	780-pin (wire bond)			445								
	780-pin				494				597	615		
	1,020-pin					698	742				773	773
	1,508-pin						951					

HardCopy structured ASIC series features

		HardCopy II (1.2 V) structured ASIC						HardCopy Stratix (1.5 V) structured ASIC				
		HC210W	HC210	HC220W	HC220	HC230	HC240	HC1S25	HC1S30	HC1S40	HC1S60	HC1S80
Density and speed	ASIC gates	1,000,000	1,000,000	1,600,000	1,600,000	2,200,000	2,200,000	–	–	–	–	–
	Additional gates for DSP blocks	0	0	300,000	300,000	700,000	1,400,000	–	–	–	–	–
	LEs	–	–	–	–	–	–	25,660	32,470	41,250	57,120	79,040
	Total RAM bits	875,520	875,520	3,059,712	3,059,712	6,368,256	8,847,360	1,944,576	2,137,536	2,244,096	5,215,104	5,658,048
	M512 RAM blocks (512 bits + 64 parity bits)	–	–	–	–	–	–	224	295	384	574	767
	M4K RAM blocks (4 Kbits[1] + 512 parity bits)	190	190	408	408	614	768	138	171	183	292	364
	M-RAM blocks (512 Kbits[1] + 65,536 parity bits)	0	0	2	2	6	9	2	2	2	6	6
	Speed grades (fastest to slowest)	–	–	–	–	–	–	–	–	–	–	–
Architectural features	Embedded processor available	Nios II						Nios II				
	DSP blocks	Implemented in HCell macros						10	12	14	18	22
	18-bit x 18-bit/9-bit x 9-bit embedded multipliers	Implemented in HCell macros						40/80	48/96	56/112	72/144	88/176
	I/O registers per I/O element	6	6	6	6	6	6	6	6	6	6	6
	True dual-port RAM	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Global and regional clock networks	16/32	16/32	16/32	16/32	16/32	16/32	36	40	40	40	40
	PLLs	4	4	4	4	8	12	6	6	6	12	12
I/O features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3						1.5, 1.8, 2.5, 3.3				
	I/O standards supported	LVDS, LVPECL, HyperTransport™, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS											
	External memory device interfaces	QDR II, DDR2, RLDRAM II, DDR, SDR						QDR II, QDR, ZBT, DDR, SDR				
	True-LVDS maximum data rate (Mbps)	125 - 1,000						840				
	True-LVDS channels (receive/transmit)	13/17	19/21	29/31	29/31	42/42	118/118	78/78	80/80	80/80	80/80	80/80
	Medium-speed LVDS data rate (Mbps) (receive/transmit)	–	–	–	–	–	–	–	2/2	10/10	36/36	46/72
	Series and differential on-chip termination	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	FPGA prototype options	EP2S30 EP2S60 EP2S90	EP2S30 EP2S60 EP2S90	EP2S30 EP2S60 EP2S90 EP2S130	EP2S60 EP2S90 EP2S130	EP2S90 EP2S130 EP2S180	EP2S180	EP1S25	EP1S30	EP1S40	EP1S60	EP1S80

[1] Kbits = 1,024 bits

FOR MORE INFORMATION

HardCopy structured ASIC series	www.altera.com/hardcopy
HardCopy II structured ASICs	www.altera.com/hardcopy2
HardCopy Stratix structured ASICs	www.altera.com/hardcopystratix
Training	www.altera.com/training

Nios II embedded processors

When you're poised to capture an early-to-market advantage with your novel idea, turn to Altera's Nios II embedded processor to give you a jump on the competition. By allowing you to drag and drop the precise mix of processors and peripherals needed to build your system, the versatile 32-bit Nios II processor equips you to create an exact-fit processor system in just minutes.

Compared with traditional embedded processors, the Nios II processor offers much more flexibility. It provides a customizable feature set, along with costs and performance that you can tailor to your unique system requirements. Used by each of the world's top 20 OEMs and with more than 15,000 development kits sold worldwide, the proven Nios II processor is the market's most popular configurable soft processor.

Nios® II

Versatility

We designed Nios II processors to meet the unique demands of new design cycles, enabling you to:

- Choose the exact set of processors, peripherals, memory, and interfaces needed for your application
- Increase system performance without changing your board design or increasing clock frequency
- Eliminate the risk of processor and ASSP obsolescence
- Lower overall system cost, complexity, and power consumption with multiple functions combined on a single chip
- Remotely upgrade your designs in the field to improve competitiveness and address changing requirements
- Target any Stratix or Cyclone series FPGA or HardCopy series structured ASIC

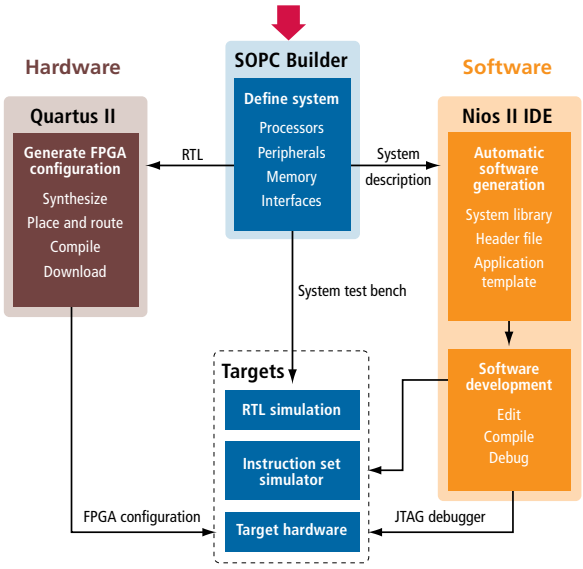
Broad software support

The Nios II processor is backed by the Eclipse-based Nios II integrated development environment (IDE) and a full range of software and operating system support provided by Altera and our partners. To boost performance, just right-click to accelerate your ANSI-C code using the Nios II C-to-Hardware Acceleration (C2H) Compiler *(see sidebar)*.

Performance

With performance clocked at well over 266 MHz, the Nios II processor is the industry's fastest FPGA-based configurable processor. You'll uncover the true processing performance potential of your FPGAs when you offload their processing tasks from software into dedicated hardware accelerators. Unlike off-the-shelf processors, FPGAs have parallel processing capabilities that let you create very high-performance, high-throughput systems.

Nios II processor development flow



Nios II C2H Compiler

An easy-to-use productivity tool, the Nios II C2H Compiler lets you boost the performance of time-critical ANSI-C functions by converting them into hardware accelerators in the FPGA. With the Nios II C2H Compiler, you can:

- **Accelerate performance of your Nios II embedded software—without increasing your clock frequency**
- **Design using the standard ANSI-C programming language and the familiar Eclipse-based Nios II IDE**
- **Boost software performance from 10x to 70x**

Traditionally, offloading software to hardware accelerators has been a manual task, benefiting only those developers with the tools, experience, and time required to create, test, and integrate register transfer level (RTL) blocks into their processor systems. The Nios II C2H Compiler automates the creation and integration of hardware accelerators, reducing development time from weeks to minutes.

Software and operating system support

	Product name	Vendor name	Description
Operating system (OS)	Nucleus PLUS	Mentor Graphics	Royalty-free, real-time OS
	MicroC/OS-II	Micrium	Real-time kernel; included in Nios II development kits
	ThreadX	Express Logic	High-performance, real-time kernel
	µClinux	Microtronix	Complete µClinux distribution for the Nios II processor
	Euros	Euros RTOS	Real-time OS
	embOS	Segger	Royalty-free real-time OS
	OSEK/VDX-OS	Vector	Preemptive multitasking operating system
	Evidence	Erika Enterprise	Real-time OS with microprocessor support
Debuggers/ IDEs	Nios II IDE	Altera Corporation	Full-featured IDE included in the Nios II Embedded Design Suite (EDS)
	EDGE IDE	Mentor Graphics	Eclipse-based IDE and debugger
	TRACE32-PowerView	Lauterbach	Flexible, fast debug environment
	Universe	Adveda	Hardware/software co-verification tools
	System Navigator	First Silicon Solutions	Software debug probe
	TRACE32-PowerView	Lauterbach	Software debug probe environment
Compilers	Tasking VX-Toolset	Altium	Optimizing C compiler
	GCC Compiler	GNU	Standard GNU compiler for Nios II processor

Nios II performance features and summary

High-performance processor core	Optimize performance-critical applications with the Nios II/f "fast" core, which has 6-stage pipeline, dynamic branch prediction, instruction and data cache, and 266+ MHz performance.
Multi-processor systems	Use multi-core systems to scale a system's performance or to break up software applications into simpler tasks. The Nios II EDS includes support for creating customized multi-core systems using Nios II processors.
High-bandwidth bus structure	Automatically generate a system interconnect fabric to support any system that you build by using the SOPC Builder system generation tool, allowing you to generate high-throughput systems supporting simultaneous multiple master/slave connections, direct memory access (DMA) channels, and on-chip data buffers.
Hardware accelerators	Use logic and memory resources in the FPGA to offload and accelerate tasks that are typically implemented in application software. You can automate this process with the Nios II C2H Compiler.
Custom instructions	Accelerate time-critical software algorithms by adding custom instructions to the Nios II processor instruction set.
Fast configurable on-chip memory	Create fixed low-latency on-chip memory buffers for performance-critical applications.

Designing with Nios II processors

Nios II processors come with a comprehensive tool suite that raises productivity by helping you and your team efficiently build and manage customized embedded processor systems. What's more, our software design suite was developed to accommodate the unique requirements of systems on a programmable chip.

Nios II EDS

The Nios II EDS is a collection of all the tools, utilities, libraries, and drivers needed to develop embedded software for the Nios II processor. Among many other tools and utilities, the Nios II EDS includes the Nios II IDE, the primary software development environment for the Nios II processor. Within this Eclipse-based GUI, you can edit, compile, download, debug, and program flash devices.

Embedded partners

Working with Altera, you'll have the backing of more than a dozen embedded partners, offering a broad range of third-party operating systems, middleware, and embedded software development tools.

Nios II Embedded Design Suite contents

- Code development tool: Nios II IDE
  - New project wizards
  - Software templates
  - Source navigator and editor
  - Compiler for C and C++ (GNU)
  - Instruction set simulator (ISS)
  - Based on the Eclipse community project
- Source debugger
- Flash programmer
  - Hardware Abstraction Layer (HAL)
  - MicroC/OS-II real-time operating system*
  - NicheStack TCP/IP Network Stack—Nios II Edition*
  - Newlib ANSI-C standard library
  - Simple file system
- Other Altera command line tools and utilities
- Design examples
- C acceleration tool: Nios II C2H Compiler*

* Production license sold separately

Hardware development tools

- Quartus II design software
- SOPC Builder, an exclusive Quartus II software tool that lets you build and evaluate systems at the block level easily and quickly
- SignalTap® II embedded logic analyzer plug-in for the Nios II processor
- FPGAView software from First Silicon Solutions for configuring and debugging Altera FPGA devices with Tektronix logic analyzers

Processor cores

The Nios II processor family consists of three CPU cores, each optimized for a specific price and performance range. All three CPU cores share a common 32-bit instruction set architecture, are binary code compatible, and are supported by the same software design suite. Simply choose which CPU is appropriate for each of your designs. You can also create multi-core systems with any Nios II CPU to scale a system's performance or to break up software applications into simpler tasks.

Nios II processor family members

Feature	Nios II/f (fast)	Nios II/s (standard)	Nios II/e (economy)
Description	Optimized for maximum performance	Balanced cost and performance	Optimized for minimum logic usage
Pipeline	6 stage	5 stage	1 stage
Multiplier	1 cycle*	3 cycle	Emulated in software
Branch prediction	Dynamic	Static	None
Instruction cache	Configurable	Configurable	None
Data cache	Configurable	None	None
Custom instructions	Up to 256	Up to 256	Up to 256

* Using DSP blocks in Stratix or Stratix II FPGAs

Embedded IP

SOPC Builder includes a portfolio of standard embedded peripherals that you can use to jump-start your system design. These IP blocks include Hardware Abstraction Layer (HAL) drivers that will let you immediately begin your software development. Visit www.altera.com/sopcready for the latest list of SOPC Builder-ready IP.

Altera embedded peripherals

• JTAG UART	• Tri-state bridge
• UART	• Serial flash controller (EPCS)
• DMA	• Ethernet
• Timer	• PLL core
• PIO	• Mailbox and mutex
• SPI	• LCD controller
• SDRAM controller	• System ID peripheral
• DDR SDRAM controller	• Performance counter
• Common flash interface controller	

Ready to go?

Make a Nios II development kit your starting point — the kits include everything you'll need to begin designing embedded systems for FPGAs:

- The processor and peripheral IP (with perpetual use license)
- Complete software development tool suite
- An FPGA development board (see the Development Kits section of this catalog for more details)

When you're ready to ship your product, you'll need a Nios II core license that's included with all Nios II development kits. You can also buy the license as a standalone offering. Contact your local Altera representative for details (ordering code: IP-NIOS; US$495). This royalty-free license never expires and allows you to target your processor design to any Altera FPGA, so your software application is preserved even if the underlying hardware changes.

Start working with the Nios II processor today using free Altera development tools. Hardware engineers should download Quartus II Web Edition design software to create Nios II processor-based hardware systems. Software designers should download the Nios II EDS to begin programming Nios II applications right away.

FOR MORE INFORMATION

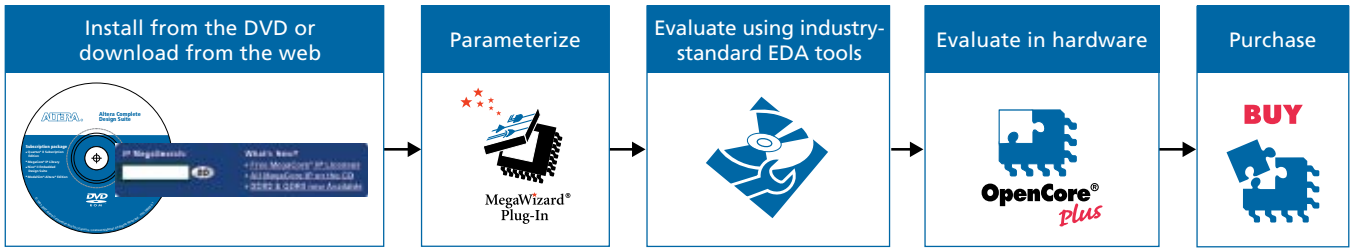
Nios II processors	www.altera.com/nios
Nios II development kits	www.altera.com/nioskits
Nios II C2H Compiler	www.altera.com/c2h
Nios user forum	www.niosforum.org
Nios wiki	nioswiki.jot.com

Intellectual property solutions

Altera offers a broad portfolio of easy-to-use IP cores. Also known as megafunctions, these IP cores are high-quality "building blocks" that you can drop into your system designs, avoiding the time-consuming task of creating complete designs from scratch. Easy-to-use, pre-verified, and configurable, Altera IP is optimized for the latest Altera devices and is fully supported in Quartus II design software. Some of the IP cores are offered by leading third-party IP vendors who have developed, optimized, and qualified their IP products for Altera devices, licensing them directly to our customers.

Discover how quickly you can use these cores to accelerate your system design, lower development costs, speed your time to market, and give your systems a competitive edge.

Altera IP design flow



Designing with Altera IP

Install	Visit the IP MegaStore website to quickly find and download megafunctions from Altera's comprehensive portfolio.
Parameterize	Use Altera's powerful, user-friendly MegaWizard® Plug-In tool to parameterize, select the right features for your needs, estimate resources, set up third-party tools, and generate all files necessary for integrating parameterized IP into your design.
Evaluate using industry-standard EDA tools	During simulation, evaluate all the features of the IP before you buy—including functionality, size, and speed in your system—with the OpenCore evaluation feature.
Evaluate in hardware	Generate time-limited FPGA programming files using the OpenCore Plus hardware evaluation feature. Then use the files to verify your complete FPGA design on your own hardware, or any other available board—all before you decide to purchase an IP license.
Purchase	When you are completely satisfied with the IP core and are ready to take your design into production, purchase the license and generate the production device programming files. Altera MegaCore® licenses are for perpetual use, support multiple projects, and include upgrades and support for one year. Floating and node-locked licenses are available for all Altera IP. Third-party IP cores are offered under a variety of different licensing terms, conditions, and pricing models. Contact the IP partners directly for details.

IP MegaStore

Visit our online IP MegaStore for a complete listing of all Altera IP. Our portfolio includes communications and I/O interconnect technologies and a broad range of cores for embedded systems and DSP applications. The website also includes information on evaluating and purchasing Altera and partner IP cores.

IP MegaStore overview

IP megafunctions	**Communications IP**	IP cores ideal for telecom, datacom, and storage applications.
	DSP IP	IP cores used for digital modulation, image, video, and high-speed DSP applications.
	Embedded processor IP	Versatile embedded processors with a wide range of peripherals, development kits, and software tools.
	Interface and peripheral IP	Extensive portfolio of standard memory and system interfaces.
Information and services	**Free IP evaluation**	Information on simulating the behavior of a megafunction within your system, verifying the functionality of your design, evaluating its size and speed, generating time-limited device programming files, and verifying the design in hardware.
	IP certifications	Overview of SOPC Builder Ready, DSP Builder Ready, and Atlantic™ Compliant certifications.
	IP licensing	Instructions on how to request a license for an Altera software product from the Altera website and have the license file sent via email complete with installation instructions.
	Documentation	Nios II embedded processor literature, MegaCore user guides, and net seminars.
	Partners	Complete listing of third-party IP providers, design service providers, embedded software, and EDA partners.

Altera megafunction library elements

Another source for Altera megafunctions is the MegaWizard Plug-in Manager within Quartus II design software. You can access an entire library of basic design elements that will support more efficient logic synthesis and device implementation. Via parameterization, you can scale the library elements in size and function. As with the individual Altera IP cores listed in the IP MegaStore, the library elements are optimized for all Altera device architectures. Learn about some of the key megafunction library elements below. Consult the MegaWizard Plug-In for the most complete listing.

Library element	Description
alt2gxb	alt2gxb, designed for use with Altera Stratix II GX and Arria GX devices, enables set-up of one or more transceivers at multiple data rates.
altmemphy	altmemphy is a physical interface which comprises silicon features as well as soft logic. It is responsible for the safe transfer of data between the FPGA and the memory, including all aspects of crossing between different clock domains.
altclkctrl	altclkctrl implements a basic clock control block.
altmemmult	altmemmult implements a multiplier.
altremote_update	altremote_update enables your designs to take advantage of dedicated remote system upgrade circuitry available in Stratix series FPGAs.
altsqrt	altsqrt implements the basic square root.
altlvds	altlvds megafunctions implement either an LVDS deserializer receiver or an LVDS serializer transmitter.
altsmi_parallel	altasmi_parallel implements a basic Active Serial Memory Interface (ASMI) block without the need to know the serial interface nature of the ASMI.
altddio	altddio megafunctions implement a DDR interface.
altpll	altpll configures the PLLs in the Stratix and Cyclone series of devices.
altfp_add_sub	altfp_add_sub implements a floating-point adder/subtractor.
altfp_div	altfp_div implements division functions.
altfp_mult	altfp_mult follows the IEEE 754 standard for floating-point multiplication.

IP megafunctions

Communications

Product name	Vendor name
Sonet/SDH	
SONET/SDH Deframer	Aliathon
SONET/SDH Demapper	Aliathon
SONET/SDH Framer	Aliathon
SONET/SDH Mapper	Aliathon
Packet Over SONET Controller	Innocor
POS-PHY Level 2 and 3 Link and PHY	Altera Corporation
SPI-4.2 Foundation and Manager	Modelware
General Framing Procedure (GFP) Controller	Innocor
Frame-mapped GFP Controller	Nuvation
GEOS-10: 10:1 Gigabit Ethernet to SONET Multiplexer	Nuvation
GEOS2+2	Nuvation
ATM Formatter	Adaptive Micro-Ware, Inc.
ATM Deformatter	Adaptive Micro-Ware, Inc.
ATM Cell Delineator	Innocor
ATM AAL5 Segmentation and Reassembly	Innocor
AAL5	Modelware
Inverse Multiplexing for ATM (IMA) version 1.0/1.1	Modelware
Bit Error Rate Tester	Innocor
UTOPIA Level 2 Master	Altera Corporation
UTOPIA Level 2 Slave	Altera Corporation
PDH	
T1 Framer	Adaptive Micro-Ware, Inc.
T1 Deframer	Adaptive Micro-Ware, Inc.
Encoding/decoding	
8B10B Encoder/Decoder	Altera Corporation
Data Encoder/Decoder	Innocor
HDLC	
HDLC, Bit-oriented	Innocor
Multi-channel HDLC	Modelware
Single-channel HDLC	Modelware
Additional functions	
CRC Compiler	Altera Corporation
SDLC Controller	CAST, Inc.
10 Gigabit Fibre Channel FC-1 Core	MorethanIP
Ethernet Layer 2 Switch	MorethanIP
BOOST Lite Bluetooth Baseband Core	Wipro - NewLogic

Digital signal processing

Product name	Vendor name
Error detection/correction	
Reed-Solomon Compiler, Decoder	Altera Corporation
Reed-Solomon Compiler, Encoder	Altera Corporation
Viterbi Compiler, High-Speed Parallel Decoder	Altera Corporation
Viterbi Compiler, Low-Speed/Hybrid Serial Decoder	Altera Corporation
Low Complexity Turbo Product Code Decoder	TurboConcept
Turbo Convolutional Decoder	TurboConcept
Turbo Product Code Decoder	TurboConcept
Very High-Speed Turbo Product Coder Decoder	TurboConcept
TC1000 WiMAX Decoder	TurboConcept
Modulation/demodulation	
FFT/IFFT	Altera Corporation
Numerically Controlled Oscillator Compiler (NCO)	Altera Corporation
Cable (QAM) Modulator	Commsonic
DVB T Modulator	Commsonic
Video and image processing	
Color Space Converter	Altera Corporation
Color Space Converter	CAST, Inc.
Image Scaler	Altera Corporation
Line Buffer Compiler	Altera Corporation
Alpha Blending Mixer	Altera Corporation
Gamma Corrector	Altera Corporation
Deinterlacer	Altera Corporation
Chroma Resampler	Altera Corporation
2D FIR	Altera Corporation
2D Medial Filter	Altera Corporation
Motion JPEG CODEC (CS6190)	Amphion Semiconductor, Ltd.
Motion JPEG Decoder (CS6150)	Amphion Semiconductor, Ltd.
Motion JPEG Encoder (CS6100)	Amphion Semiconductor, Ltd.
Fast Black and White JPEG Decoder	Barco Silex
Fast Color JPEG Decoder	Barco Silex
JPEG2000 Decoder	Barco Silex
JPEG2000 Encoder	Barco Silex
JPEG CODEC	CAST, Inc.
JPEG Decoder	CAST, Inc.
JPEG Encoder	CAST, Inc.
Forward Discrete Wavelet Transform (FDWT)	Barco Silex
Inverse Discrete Wavelet Transform (IDWT)	Barco Silex
H.264 Loop Filter	ATEME
H.264 CABAC/CAVLC Bitstream Generator	ATEME

IP megafunctions (continued)

	Product name	Vendor name
Digital signal processing (continued)	**Video and image processing (continued)**	
	H.264 SD MPEG-4 AVC Encoder	ATEME
	H.264 HD MPEG-4 AVC Encoder	ATEME
	H.264 MPEG-4 AVC SD/HD Encoder	CAST, Inc.
	MPEG2 Decoder	Amphion Semiconductor, Ltd.
	Additional functions	
	CIC Compiler	Altera Corporation
	FIR Compiler	Altera Corporation
	2D DCT IDCT	Barco Silex
	Forward Discrete Cosine Transform (DCT)	CAST, Inc.
	SHA-1	CAST, Inc.
	AES Cryptoprocessor	CAST, Inc.
	DES Cryptoprocessor	CAST, Inc.
	High-Speed AES Encryption/ Decryption Cores	D'Crypt Pte. Ltd.
	Accelerated Display Graphics Engine	Bitsim
	Floating Point Arithmetic Unit	Digital Core Design
	Floating Point Mathematics Unit	Digital Core Design
	Floating Point Pipelined Divider Unit	Digital Core Design
	Floating Point to Integer Pipelined Converter	Digital Core Design
Embedded processors	Nios II Embedded Processor	Altera Corporation
	Avalon FIFO Memory Component	Altera Corporation
	Avalon MM Pipeline Bridge	Altera Corporation
	Avalon MM Clock-Crossing Bridge	Altera Corporation
	Avalon MM Compact Flash Interface	Altera Corporation
	Avalon MM DMA Controller	Altera Corporation
	Avalon MM Ethernet Port (SMSC LAN91C111 MAC/PHY)	Altera Corporation
	Avalon MM Flash	Altera Corporation
	Avalon MM Interval Timer	Altera Corporation
	Avalon MM JTAG UART	Altera Corporation
	Avalon MM On-chip ROM and RAM	Altera Corporation
	Avalon MM Parallel I/O (PIO)	Altera Corporation
	Avalon MM Serial Peripheral Interface (SPI)	Altera Corporation
	Avalon MM SRAM	Altera Corporation
	Avalon MM SSRAM	Altera Corporation
	Avalon Streaming Components and Adaptors	Altera Corporation
	Avalon MM UART	Altera Corporation
	Scatter/Gather DMA	Altera Corporation
	8-bit Microcontroller, 8051	CAST, Inc.
	R8051 Microcontroller	CAST, Inc.

	Product name	Vendor name
Embedded processors (continued)	DR8051 8-Bit RISC Microcontroller	Digital Core Design
	DR8052EX 8-Bit RISC Extended Microcontroller	Digital Core Design
	C68000 Microprocessor	CAST, Inc.
	CZ80CPU Processor	CAST, Inc.
	R80515 Microcontroller	CAST, Inc.
	DF6811CPU 8-Bit Microcontroller CPU	Digital Core Design
	DFPIC1655X RISC Microcontroller	Digital Core Design
Interfaces and peripherals	**PCI**	
	PCI Express x1, x4, and x8 Lane	Altera Corporation
	PCI Express	PLDApplications
	PCI-X Master/Target Core 32/64-Bit	PLDApplications
	PCI Compiler, 32-bit Master/Target	Altera Corporation
	PCI Compiler, 32-bit Target	Altera Corporation
	PCI Compiler, 64-bit Master/Target	Altera Corporation
	PCI Compiler, 64-bit Target	Altera Corporation
	Scatter Gather DMA Controller	Altera Corporation
	32-Bit PCI Bus Master/Target Interface	Eureka Technology Inc.
	32-Bit PCI Bus Target Interface	Eureka Technology Inc.
	32-bit PCI Host Bridge	Eureka Technology Inc.
	64-bit PCI Bus Master/Target Interface	Eureka Technology Inc.
	64-bit PCI Bus Target Interface	Eureka Technology Inc.
	64-Bit PCI Host Bridge	Eureka Technology Inc.
	Integrated PCI Core	Northwest Logic, Inc.
	PCI Interface	Northwest Logic, Inc.
	32/64-Bit PCI Bus Master/Target Interface, 33/66 MHz	PLDApplications
	32/64-Bit PCI Bus Target Interface, 33/66 MHz	PLDApplications
	AMBA-AHB PCI Bridge	PLDApplications
	PCI Bus Arbiter	Eureka Technology Inc.
	PCI-ISA Bridge	Eureka Technology Inc.
	PCI-PCI Bridge	Eureka Technology Inc.
	Ethernet	
	Tri-Speed Ethernet MAC	Altera Corporation
	10 Gigabit Ethernet MAC	MorethanIP
	10 Gigabit Ethernet Physical Coding Sublayer (PCS)	MorethanIP
	MAC-1G Gigabit Ethernet MAC	CAST, Inc.
	Gigabit Ethernet MAC	IFI
	High-Performance Gigabit Ethernet MAC	IFI
	10/100/1000 1588 Ethernet MAC	MorethanIP

IP megafunctions (continued)

Interfaces and peripherals (continued)

Product name	Vendor name
Ethernet (continued)	
10/100/1000 Ethernet MAC with SGMII	MorethanIP
10/100/1000 Ethernet MAC-Net	MorethanIP
10/100/1000 Mbps Full Duplex Ethernet MAC	MorethanIP
AnySpeed Ethernet MAC	MorethanIP
10/100 Ethernet MAC	MorethanIP
I2C/CAN	
I2C Bus Controller	CAST, Inc.
I2C Bus Controller Slave	CAST, Inc.
DI2CM I2C Bus Interface-Master	Digital Core Design
DI2CSB I2C Bus Interface-Slave	Digital Core Design
I2C Master and Slave	Microtronix Inc.
C_CAN	Bosch
CAN	CAST, Inc.
Nios_CAN	IFI
Nios II Advanced CAN	IFI
Memory controllers	
DDR and DDR2 SDRAM Controllers	Altera Corporation
DDR and DDR2 High Performance SDRAM Controllers	Altera Corporation
DDR2 SDRAM Controller	Northwest Logic, Inc.
QDR II SRAM Controller	Altera Corporation
RLDRAM II Controller	Altera Corporation
DMA Controller	Eureka Technology Inc.
DMA Controller for AHB	Eureka Technology Inc.
Pipeline SDRAM Controller	Eureka Technology Inc.
FCRAM Controller	Northwest Logic, Inc.
SDR SDRAM Controller	Northwest Logic, Inc.
Additional interfaces	
ASI	Altera Corporation
HyperTransport™	Altera Corporation
HyperTransport 16-Bit	GDA Technologies
Serial RapidIO	Altera Corporation
SD/HD SDI	Altera Corporation
Audio Embed Mux/Demux for SDI	Gennum Corporation

Interfaces and peripherals (continued)

Product name	Vendor name
Additional interfaces (continued)	
SerialLite II	Altera Corporation
Multi-Gigabit Fibre Channel Transport Core	MorethanIP
ATA-4 Host Controller	Nuvation
ATA-5 Host Controller	Nuvation
Serial ATA Host Controller	Nuvation
MediaLB Device Interface	IFI
Peripherals	
1394A Firewire	CAST, Inc.
CUSB USB Function Controller	CAST, Inc.
CUSB2 USB High-Speed Function Controller	CAST, Inc.
USB Function Controller	SLS
H16450 UART	CAST, Inc.
H16450S UART	CAST, Inc.
H16550 UART	CAST, Inc.
H16550S UART	CAST, Inc.
D16550 UART with 16 Bytes FIFO	Digital Core Design
H16750 UART	CAST, Inc.
H16750S UART	CAST, Inc.
UART	Eureka Technology Inc.
GPIO8-APB	CAST, Inc.
H8250	CAST, Inc.
Programmable Interval Timer/ Counter, 8254	CAST, Inc.
MD5	CAST, Inc.
NAND Flash Memory Conroller - nflashctrl	CAST, Inc.
Smart Card Reader	CAST, Inc.
ISA/PC Card/PCMCIA/Compact Flash Host Adapter	Eureka Technology Inc.
DSPI Serial Peripheral Interface Master/Slave	Digital Core Design
SD/MMC SPI	El Camino GmbH
OBSAI RP3	Elektrobit
PowerPC Bus Arbiter	Eureka Technology Inc.
PowerPC Bus Master	Eureka Technology Inc.
PowerPC Bus Slave	Eureka Technology Inc.
PowerPC to PCI Host Bridge	Eureka Technology Inc.
PowerPC/SH/1960 System Controller	Eureka Technology Inc.

FOR MORE INFORMATION Intellectual property www.altera.com/ipmegastore

Quartus II design software

If you're looking for a design environment that will quickly move you from concept to creation, choose Altera's Quartus II design software. Number one in performance and productivity for CPLD, FPGA, and structured ASIC designs, Quartus II software offers complete, automated system definition and implementation, all without requiring lower-level HDL or schematics. This capability—plus its seamless integration with leading EDA software tools and flows—will help turn your ideas into working systems in minutes.

Quartus II software

	Subscription Edition	Web Edition
Devices:	All	MAX and Cyclone series; Arria GX family
Features:	100%	95%
Distribution:	Download and DVD	Download and DVD
Cost:	Paid license	Free license
Operating system support:	Windows, UNIX, Linux	Windows

Quartus II design software features summary

Design flow methodology	**Incremental compilation**	Improves design timing closure and reduces design compilation times up to 70 percent. Supports team-based design.
	Up-front I/O assignment and validation	Enables PCB layout to begin earlier.
	Pin planner	Eases the process of assigning and managing pin assignments for high-density and high pin-count designs.
	SOPC Builder	Automates adding, parameterizing, and linking IP cores—including embedded processors, coprocessors, peripherals, memories, and user-defined logic.
	Off-the-shelf IP cores	Lets you construct your system-level design using IP cores from Altera's megafunction library and from Altera's third-party IP partners.
	Parallel development of FPGA prototypes and structured ASICs	Allows for FPGA prototypes and HardCopy structured ASICs to be designed in parallel using the same design software and IP.
	Scripting support	Supports command-line operation and Tcl scripting, as well as GUI design processing.
Performance and timing closure methodology	**Physical synthesis optimization**	Uses post place-and-route delay knowledge of a design to improve performance.
	Design space explorer	Increases performance by automatically iterating through combinations of Quartus II software settings to find optimal results.
	Extensive cross-probing	Unmatched support for cross-probing between verification tools and design source files.
	Optimization advisors	Provides design-specific advice to improve design timing performance, resource usage, and power consumption.
	Timing closure floorplan editor	Enables analysis of timing data in the floorplan.
	Chip planner	Reduces verification time (while maintaining timing closure) by enabling small, post place-and-route design changes to be implemented in minutes.
	RTL viewer and technology map viewer	Provides schematic representation that can be used to analyze a design's structure before and after its implementation.
Verification	**TimeQuest timing analyzer**	Create, manage, and analyze complex timing constraints, and quickly perform advanced timing verification with TimeQuest, an ASIC-strength timing analysis tool with native SDC support.
	SignalTap II embedded logic analyzer	Supports the most channels, fastest clock speeds, largest sample depths, and most advanced triggering capabilities available in an embedded logic analyzer.
	PowerPlay technology	Enables you to accurately analyze and optimize both dynamic and static power consumption.
	SignalProbe routing	Routes an internal node to an unused or reserved pin for analysis with an external scope or logic analyzer.
Third-party support	**EDA partners**	Offers EDA software support for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification.

Free Quartus II Web Edition software

Our free Quartus II Web Edition software for Windows-based PCs includes everything you need to design for Altera's latest CPLD and low-cost FPGA families, as well as our new Arria GX FPGA family. Quartus II Web Edition software also includes support for entry-level members of Altera's high-end FPGA families.

Quartus II Web Edition features include:

- Schematic- and text-based design entry
- Integrated VHDL and Verilog HDL synthesis and support for third-party synthesis software
- SOPC Builder system generation software
- Placement, routing, verification, and programming functions
- Mentor Graphics® ModelSim®–Altera Web Edition simulation software (limited-time offer)
- TimeQuest timing analyzer, an ASIC-strength timing analysis tool
- Installation and evaluation of the Altera MegaCore IP library
- Support for Windows

Altera subscription program

Altera's subscription program offers a comprehensive suite of premium software and IP products. Included in the subscription are:

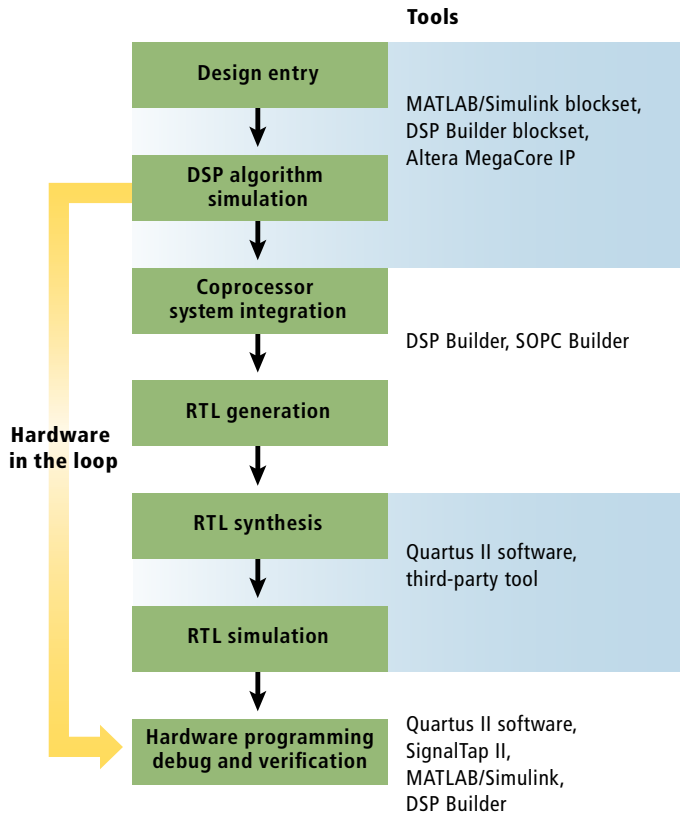
- Quartus II Subscription Edition software
  - Support for all Altera devices and software features
  - Support for Windows, UNIX, and Linux operating systems
- Nios II EDS
- ModelSim®–Altera edition simulation software
- Complete IP base suite, which includes full licenses to the following Altera functions:
  - FIR Compiler
  - NCO Compiler
  - FFT Compiler
  - DDR SDRAM Controller
  - DDR SDRAM High Performance Controller
  - DDR2 SDRAM Controller
  - DDR2 SDRAM High Performance Controller
  - QDR II SRAM Controller
  - RLDRAM II Controller
  - SerialLite II

Download the latest software and IP in the Altera subscription program at www.altera.com/download.

DSP Builder

DSP Builder is a digital signal processing (DSP) development tool that interfaces between the Quartus II software and The MathWorks MATLAB/Simulink tools. DSP system design in Altera PLDs requires high-level algorithm and HDL development tools. Altera's DSP Builder integrates these tools by combining the algorithm development, simulation, and verification capabilities of The MathWorks MATLAB and Simulink system-level design tools with VHDL synthesis, simulation, and Altera development tools. DSP Builder shortens DSP design cycles by helping you create the hardware representation of a DSP design in an algorithm-friendly development environment.

DSP design flow overview



DSP Builder features summary

The MathWorks MATLAB and Simulink support	Links The Mathworks MATLAB (signal processing toolbox and filter design toolbox) and Simulink software with Altera Quartus II software.
SignalTap II logic analyzer support	Probes signals from the Altera device on the DSP board and imports the data into the MATLAB work space to facilitate visual analysis.
SOPC Builder and Nios II support	Includes blocks that you can use to build custom logic that works with Nios II embedded processors and other Quartus II SOPC Builder designs.
Testbench generation	Automatically generates a VHDL testbench or Quartus II Vector File (.vec) from MATLAB and Simulink test vectors.
Simulation support	Enables bit- and cycle-accurate design simulation.
Hardware in the loop	Accelerates system-level co-simulation with Simulink and provides advanced debugging features.

SOPC Builder

SOPC Builder is an exclusive Quartus II software tool that enables you to quickly and easily build and evaluate systems at the block level. Using SOPC Builder, you can focus on your custom user logic design, differentiating functions by eliminating manual system integration tasks. In addition to your custom logic, you can select common functions from the Altera or Altera partner IP core libraries to include in your system. SOPC Builder automatically generates interconnect logic to make the system work optimally and creates a testbench to verify functionality, saving valuable design time.

Peripheral expansion of stand-alone processors

SOPC Builder includes a component editor feature so you can easily interface to nearly any external processor or DSP device. If you create an SOPC Builder component interface to your processor, you can add additional I/O pins, prepackaged peripherals, or custom, self-made peripherals in just a few mouse clicks. SOPC Builder will build the system and output header files for your software development team. Your team can then access the peripherals from the external processor using their preferred integrated development environment.

Connection to ASSPs or CPUs via PCI

Many ASSPs and processors include PCI interfaces. Altera's SOPC Builder and the SOPC Builder Ready PCI Compiler function let you easily build systems that communicate through PCI to these ASSPs or external processors.

SOPC Builder features summary

IP selection and parameter selection	Select and parameterize off-the-shelf IP from Altera and our partners or create your own custom components. Off-the-shelf IP includes the Nios II processor, memory interfaces, common embedded system peripherals, bridges and interfaces, DSP IP, and hardware accelerator peripherals.
System interconnect fabric generation	Uses an optimal interconnect fabric created specifically for the requirements of each system. Integration tasks automatically performed by SOPC Builder include: • Data-path multiplexing between design blocks • Address decoding • Wait-state generation • Dynamic bus sizing • Interrupt priority assignment • Clock domain crossing to connect peripherals or systems operating on different clock domains
Component editor	Allows you to create your own custom SOPC Builder components.
IP reuse	Reuse any custom-created IP core designed for SOPC Builder in future products.
Testbench generation	Outputs testbench suites to test-generated systems.
Header file generation	Outputs a custom header file based on the memory map and components of the generated system.

FOR MORE INFORMATION

Quartus II software	www.altera.com/quartus2
Quartus II Web Edition and Subscription Edition download	www.altera.com/download
Purchase Quartus II	www.altera.com/buysoftware
Quartus II literature	www.altera.com/literature
Training	www.altera.com/training

Development kits

To help you simplify your design process and reduce time-to-market, Altera and our partners offer an array of feature-rich development kits. These kits speed system design by providing you with test and debug platforms for RTL generation, while also allowing you to start developing your application software. With reference designs, cables, and programming hardware, these kits provide an ideal FPGA or CPLD design environment.

New to Altera's technologies? Or a seasoned veteran? Either way, our development kits were created to be easy to master, delivering detailed example designs supporting Quartus II design software, IP design flow, and programming options for Altera devices. What's more, these kits provide a platform for you to use the Altera IP simulation and hardware evaluation flow. Read on to learn more about the different types of development kits that you can plug into your design process.

DSP development kits

Prototype and debug DSP designs for programmable logic using Altera DSP development kits. These kits include all of the critical design resources you'll need: a DSP development board populated with an Altera FPGA, Quartus II software (one-year, time-limited license), DSP Builder (Quartus II MATLAB/Simulink interface), a 30-day evaluation copy of MATLAB/Simulink, and system reference designs. In addition, by using the hardware evaluation feature of our DSP IP, you can jump-start your designs for video and image, wireless, and other complex digital communications by implementing entire subsystems in hardware within hours.

I/O interconnect development kits

Altera and our partners offer cost-effective development kits to evaluate high-speed interfaces. Consider, as an example, the Transceiver Signal Integrity Development Kit, Stratix II GX Edition. This kit enables you to verify our embedded transceiver for use with a wide variety of interfaces such as PCI Express, Gigabit Ethernet, XAUI, Fibre Channel, Serial RapidIO, HD-SDI, and other major standards. Altera's PCI development kits are another example. These kits provide a flexible hardware platform to test and validate your PCI-based design. Featuring a variety of memory, interfaces, and peripherals on the standard PCI card form factor, the PCI development kits offer a complete design environment supporting 32- or 64-bit, 33- or 66-MHz PCI, PCI-X, and PCI Express operations.

Each I/O interconnect board comes with a one-year license to Quartus II design software, a user application, and a library of reference designs. You can also use the development kits and hardware IP evaluation to assess a variety of high-speed interconnect IP cores as well as to rapidly prototype and debug in a real-time environment.

Embedded development kits

For embedded processor system development, look no further than Altera's embedded development kits. The Altera Nios II development kits include Nios II embedded processors and a perpetual license to create embedded systems, the Nios II Embedded Design Suite (EDS), and access to more than 60 peripheral IP cores. The kits contain Quartus II design software (one-year, time-limited license), a feature-rich FPGA-based development board (including power supply, USB Blaster™ download cable, and LCD display), extensive reference designs, tutorials, and complete documentation. In addition, numerous partners are offering companion boards enabling application-specific embedded Nios II development.

Nios II Development Kit, Stratix Edition

General-purpose development kits

Whether designing with our MAX II or MAX CPLDs, Cyclone series FPGAs, or Stratix or Stratix GX FPGA family devices, you can get off the ground quickly with our portfolio of low-cost, easy-to-use development kits. For example, the MAX II Development Kit provides a complete design environment with all of the software, cables, and accessories needed to evaluate the MAX II feature set or begin prototyping a design before you've received custom hardware. These kits enable increased design productivity whether you're evaluating one of the devices, validating your design, prototyping, or using FPGAs as part of your ASIC prototyping strategy. Tap into the wide variety of general purpose FPGA and CPLD development kits from Altera and our partners.

Development kits

DSP

Product name and vendor name	Device	Features
Cyclone III DSP Developers Kit* [DK-DSP-3C120N] **Altera Corporation**	Cyclone III EP3C120N	This kit is for general DSP or wireless design engineers, regardless of whether you need pre-processing, DSP plus FPGA co-processing, or post-processsing. Complete high-speed analog-to-digital and digital-to-analog conversion capability (16-bit, 200 Ms/s) is included as well as interfaces to DM642 and DaVinci. Altera's DSP Builder GUI simplifies the information flow between the FPGA toolset and MATLAB/Simulink (30-day eval copy included).
Cyclone III Video & Image Processing Development Kit* [DK-VIP3C120N] **Altera Corporation**	Cyclone III EP3C120N	This kit is designed to help you start developing complex video applications. It supports various video I/O interfaces, allowing you to get your video data in and out of the Cyclone III FPGA. Different video interfaces are supported using the different daughtercards included in this kit: cards supporting ASI/SDI, composite, component, and DVI interfaces.
Video Development Kit, Cyclone II Edition* [DK-VIDEO-2C70N] **Altera Corporation**	Cyclone II EP2C70N	Composite video input channels (NTSC/PAL), 10-bit BT.656 output, 2 x 2 14-bit, 125 MSPS A/D, 2 x 14-bit, 165 MSPS D/A, VGA DAC, stereo audio CODEC (96 KHz), EMIF connector, Mictor connector, expansion connector, 256-Mbit DDR2 DIMM, 1-Mbit synchronous SRAM, 2 x EPCS64 devices, MATLAB/Simulink evaluation software, DSP Builder development tool.
Sendero Imaging & Consumer Evaluation Kit **AleaREP**	Cyclone II EP2C35	A low-cost evaluation board demonstration and evaluation platform for imaging and consumer applications. Includes a PCIe 1-lane Philips PHY.
Raven D **MangoDSP**	Cyclone FPGAs	Offers a scalable platform for high-performance video capture, processing, streaming, storage and retrieval; ideal for use in video surveillance systems. Interfaces include 4 composite video inputs, 1 composite video out, 2 audio inputs with microphone or line amplifiers, 2 audio line outputs, 4 relay contacts, and 8 alarm TTL compatible inputs.
TREX-C1 Development Board **Terasic Technologies Inc.**	Cyclone EP1C6	Embedded system development kit; peripheral set includes USB-Blaster cable, audio, VGA, flash memory, SDRAM, and CF socket; many reference designs with free source code.
DSP FPGA Coprocessing Development Platform **ATEME**	Cyclone EP1C20	An all-in-one bundle enabling fast development of mixed designs, using both FPGA and DSP.
DSP Development Kit, Stratix II Edition* [DK-DSP-2S60N] **Altera Corporation**	Stratix II EP2S60N	2-channel 12-bit, 125 MSPS A/D, 2-channel 14-bit 165 MSPS D/A, VGA DAC, stereo audio CODEC 96 KHz, connector for TI C6000 kit, two 40-pin connectors for analog devices A/D boards, Mictor connector, RSD232 serial port, RJ45, 32-Mbyte SDR SDRAM, 16-Mbyte flash, 1-Mbit SRAM, 16-Mbyte compact flash, MATLAB/ Simulink evaluation software, Quartus II development kit edition (DKE) software, DSP Builder development tool, evaluation DSP IP cores, system reference designs and labs, Nios II reference designs.
DSP Development Kit, Stratix II Professional Edition* [DK-DSP-2S180N] **Altera Corporation**	Stratix II EP2S180N	2-channel 12-bit, 125 MSPS A/D, 2-channel 14-bit 165 MSPS D/A, VGA DAC, stereo audio CODEC 96 KHz, connector for TI C6000 kit, two 40-pin connectors for Analog Devices A/D boards, Mictor connector, RSD232 serial port, RJ45, 32-Mbyte SDR SDRAM, 16-Mbyte flash, 1-Mb SRAM, 16-Mbyte compact flash, MATLAB/Simulink evaluation software, Quartus II DKE, DSP Builder development tool, evaluation DSP IP cores, system reference designs and labs, Nios II reference designs.
Audio Video Development Kit, Stratix II GX Edition* [DK-VIDEO-2SGX90N] **Altera Corporation**	Stratix II EP2SGX90N	DVI inputs/outputs, SD/HD/SDI inputs/outputs, ASI inputs/outputs, AES3 and S/PDIF audio interfaces, DDR2 DIMM, 2-Mbyte SRAM, HSMC expansion connector, 10/100/1000 Ethernet PHY, 1394 MAC/ PHY, USB MAC/PHY, Video and Image Processing Suite evaluation IP cores, SDI reference design.
Bluejay CPCI **MangoDSP**	Stratix II EP2S130 (4 devices)	A CPCI 6U video and imaging board for applications requiring the highest processing power.

* RoHS compliant (lead free)

Development kits (continued)

	Product name and vendor name	Device	Features
DSP (continued)	B2-AMC Universal Baseband Processing Module **BittWare**	Stratix II FPGAs	Stratix II FPGA, TigerSHARC DSP cluster, full-height, single-wide AMC, configurable to support Serial RapidIO, PCI Express, GbE, and XAUI.
	GT-3U-cPCI CompactPCI Board **BittWare**	Stratix II GX EP2SGX90	Ruggedized hybrid signal processing, Stratix II FPGA, TigerSHARC DSP cluster, BittWare's ATLANTIS architecture providing 2 Gbytes/s of external I/O throughput, DDR2 SRAM/QDR SDRAM, flash memory.
	TS PCI A25/A40 Imaging Tool Kit **GE Fanuc**	Stratix EP1S25	TS-Camera Link® Development Kits provide an easy-to-use Camera Link Interface and Wave Imaging Toolkit on a powerful FPGA-based computing platform.
	TS PMC Video Development Kit **GE Fanuc**	Stratix EP1S40	A TS-PMC commercial board, TS-RS170 video mezzanine I/O, for video imaging applications.
	TS Software Defined Radio Development Kits **GE Fanuc**	Stratix EP1S80	Development kit for software-defined radio, radar, sonar, and other high-performance signal processing applications.
	Harrier CPCI **MangoDSP**	Stratix FPGAs	A video processing card ideal for DSP applications such as medical imaging, high-resolution optical inspection, third-generation base stations, and advanced military applications supporting up to 16 DSPs and 5 FPGAs providing over 100 billion operations per second. Nearly 2 Gbytes of on-board memory is also included.
	Seagull PCI **MangoDSP**	Stratix EP1S20	A programmable solution for video and imaging applications that includes 4 Stratix FPGAs with 8 DSP and ready-to-use video libraries.
	PM430/431 PMC FPGA Processing Module **Parsec**	Stratix EP1S25 to EP1S40	Single/dual PMC module, processing FPGA(s), external ZBT memory, high-speed DSP processing, high-bandwidth data transfer, Windows and MATLAB driver, FFT reference design.
	Video Input Daughter Card [DC-VIDEO-TVP5146] **Altera Corporation**	Daughtercard	2 composite video input channels using TI ADC, support for NTSC/PAL, 10-bit BT.656 output, compatibility with expansion connector found on most Altera development kits; included with Video Development Kit, Cyclone II Edition.
	SC DVI Output Module **Bitec**	Daughtercard	Supports all Altera development kits with Altera DVI expansion slots.
I/O Interconnect	PCI Development Kit, Cyclone II Edition* [DK-PCI-2C35N] **Altera Corporation**	Cyclone II EP2C35N	Short-form universal PCI (3.3 or 5.0 V) card (32/64-bit, 33/66 MHz), 128-Mbit DDR2 SDRAM, 2 x EPCS64 devices, 100-MHz oscillator, SMA/PCI connector clock input, 4 x user push-button switches, 8 x DIP switch, 8 x user LEDs.
	Cyclone II PCI Express Development Kit* [DK-PCI-2C35N] **Knott Systems**	Cyclone II EP2C35N	Provides a hardware platform for developing and prototyping PCI Express, DDR2 SDRAM, and the 10/100/1000 Ethernet interface.
	1-Lane PCI Express Board **HiTech Global**	Cyclone II EP2C50	One-lane, low-cost PCI Express development platform.
	4-Lane PCI Express Board **HiTech Global**	Cyclone II EP2C70	Four-lane PCI Express development board with external PHY.
	PCI Express Design Kit with Cyclone II + External PHY **PLDApplications**	Cyclone II EP2C20 to EP2C50	Designed to support low-cost Altera FPGA families, includes free board version of PLDA's IP Core for PCIe and a Phillips PCIe x1 PHY.
	PCI Express Development Kit, Stratix II GX Edition* [DK-PCIE-2SGX90N] **Altera Corporation**	Stratix II GX EP2SGX90N	PCI Express IP core (eval), 2 x HSMC connectors, 10/100/1000 Ethernet PHY, 2 x SFP interfaces, 256-Mbit DDR2 SDRAM, 2-Mbit QDR II SRAM, 64-Mbyte flash.
	PCI XpressGXII Board **PLDApplications**	Stratix II GX EP2SGX90	Includes free PCI Express IP core, x1, x4, x8 configurations, FPGA-based, x8 PCI Express male connector, endpoint PCI Express designs.
	8-Lane PCI Express Board **HiTech Global**	Stratix II GX EP2SGX90 and EPS2SGX130	Eight-lane PCI Express development platform (endpoint).
	Transceiver Signal Integrity Development Kit, Stratix II GX Edition* [DK-SI-2SGX90N] **Altera Corporation**	Stratix II GX EP2SGX90N	Six full-duplex transceiver channels with SMA connectors, one microstrip channel, four matched stripline channels, 25-MHz and 156.25-MHz clock oscillators, SMA clock input, 6 x user push-button switches, 8 x DIP switches, 8 x user LEDs, 2 x 7-segment displays, USB port.

* RoHS compliant (lead free)

Development kits (continued)

	Product name and vendor name	Device	Features
I/O Interconnect (continued)	PCI X/PCI Development Kit (PCIXSYS2) **PLDApplications**	Stratix II EP2S60 to EP2S180	Ideally suited for ASIC/FPGA prototyping, data acquisition applications.
	DN7000K10PCIS **The Dini Group**	Stratix II EP2S90, EP2S130, or EP2S180	Complete logic element system providing ASIC or IP designers with a vehicle to cost effectively prototype logic and memory design.
	PCI/PCI-X Board **HiTech Global**	Stratix II EP2S90 and EP2S180	PCI/PCI-X development platform.
	PCI Express Design Kit with Stratix GX (x1, x4) **PLDApplications**	Stratix GX EP1SGX40	Includes free PCI Express IP core (board license), available for ASIC and FPGA design flows, endpoint, root port and bridge, and technical support.
	4-Lane PCI Express Kit **HiTech Global**	Stratix GX EP1SGX40	Four-lane low-cost PCI Express design kit.
	8-Lane PCI Express Board **HiTech Global**	Stratix GX EP1SGX40	Eight-lane PCI Express, PCI, and PCI-X development platform.
	PCI/PCI-X Board **HiTech Global**	Stratix EP1S10F780, EP1S20F780, EP1S25F780, and EP1S30F780	PCI/PCI-X development platform.
	Q5V4 Series FPGA Development Boards **Rowe Engineering**	Stratix EP1S30 to EP1S80	Easy-to-use family of prototype boards incorporating up to 4 Altera Stratix devices.
	PCI X/PCI Development Kit (PCIXSYS) **PLDApplications**	Stratix EP1S10 to EP1S40	Includes free PCI-X / PCI IP core, high-performance framegrabber PCI form factor, or standalone box, scalable hardware architecture.
	802.11b Wireless Design Kit **Microtronix Inc.**	Daughtercard	Kit includes a wireless 802.11b CompactFlash card and a Microtronix CompactFlash board.
	Ethernet USB Expansion Kit **Microtronix Inc.**	Daughtercard	Kit includes a wireless 802.11b CompactFlash card and a Microtronix CompactFlash board.
	I2C Design Kit **Microtronix Inc.**	Daughtercard	Provides an easy way to design, develop and text the Microtronix I2C IP core.
	10/100/1000 Ethernet PHY Daughter Board with Marvell PHY **MorethanIP**	Daughtercard	Provides the ability to implement high-speed Ethernet PHY solutions for prototyping and evaluation and embedded software development.
	10/100/1000 Ethernet PHY Daughter Board with National Semiconductor PHY **MorethanIP**	Daughtercard	Provides the ability to implement Fast Ethernet solutions for prototyping and evaluation and embedded software development.
Embedded	Cyclone III Embedded Evaluation Kit* [DK-EMB-3C25N] **Altera Corporation**	Cyclone III EP3C25N	Beginners can check out the pre-built, eye-catching demos displayed on the LCD touch panel screen, or do some light-weight development. Advanced microcontroller designers can learn about the "hottest" techniques, multi-processor systems, hardware acceleration using Nios C2H Compiler, or designing a complete system in 30 minutes. The kit includes a complete hardware and software design environment for 32-bit microcontroller plus FPGA evaluation.
	Nios II Development Kit, Cyclone III Edition* [DK-NIOS-3C120N] **Altera Corporation**	Cyclone III EP3C120N	Altera's Nios II family of embedded processor-based development kits, the top selling type of kit sold in the last few years, has been outfitted with the latest in cutting-edge hardware and software technology. The unique combination of high-performance embedded processor power and easy-to-use integrated design software has been updated to take advantage of Cyclone III devices, the industry's lowest cost, first-to-market 65-nm FPGA family. This development kit provides an ideal environment for developing and prototyping a wide range of price-sensitive, high-performance embedded applications.
	Nios II Development Kit, Cyclone II Edition* [DK-NIOS-2C35N] **Altera Corporation**	Cyclone II EP2C35N	Perpetual Nios II license, µC-OSII evaluation version, 1-Mbit SRAM, 16-Mbit SDR SDRAM, 16-Mbit flash, CompactFlash connector header, 10/100 Ethernet MAC/PHY, 2 x RS-232, expansion headers, debug Mictor connector, 4 x button switches, 8 x LEDs, 2 x 7-segment LED display.

* RoHS compliant (lead free)

Development kits (continued)

	Product name and vendor name	Device	Features
Embedded (continued)	Firefly Modules EP2C20, EP2C35 and EP2C50 editions* **Microtronix Inc.**	Cyclone II EP2C20, EP2C35 and EP2C50	Complete Nios II processor system on a module, up to 95 user I/O available, functionally compatible with Firefly I modules, hardware DSP support.
	Product Starter Kit EP1C4 **Microtronix Inc.**	Cyclone EP1C4	Features SDRAM and flash memory for running uClinux, 88 user I/O available for carrier board peripherals, RS-232 serial device interface, low profile, 0.1" male headers.
	SOCkit Cyclone EP1C6 NIOS/LVDS Evaluation Kit **Dallas Logic**	Cyclone EP1C6	Nios II processor system that includes SSRAM, flash, SD/MMC slot, and RS232 connectors.
	DIGILAB CC Development Kit **El Camino GmbH**	Cyclone EP1C20	Flexible and powerful development platform ideal for evaluating Altera Cyclone device features as well as analyzing high-speed LVDS communication and DSP algorithm development.
	Product Starter Kit EP1C12 **Microtronix Inc.**	Cyclone EP1C12	Features SDRAM and flash memory for running uClinux, 88 user I/O available for carrier board peripherals, RS-232 serial device interface, low profile, 0.1" male headers.
	Nios II Development Kit, Stratix II Edition* [DK-NIOS-2S60N] **Altera Corporation**	Stratix II EP2S60N	Perpetual Nios II license, µC-OSII evaluation version, 1-Mbit SRAM, 16-Mbit SDR SDRAM, 16-Mbit flash, CompactFlash connector header, 10/100 Ethernet MAC/PHY RJ45, RS-232, 2 expansion headers, debug Mictor connector, 2 expansion/prototype headers, Quartus DKE, Nios II Embedded Design Suite.
	DIGILAB CX II **El Camino GmbH**	Stratix II EP2S90, EP2S130, or EP2S180	Stratix II development board, stackable with 4 SSRAM banks, serial flash, security key supported SD/MMC socket, and 56 user I/O pins.
	PMC Stratix Development Kit **Rapid Technology**	Stratix EP1S25	High-performance computing subsystem and I/O expansion module for embedded applications in PMC form factor.
	DIGILAB CX **El Camino GmbH**	Stratix EP1S40, EP1S60, or EP1S80	Stratix development board, stackable with 2 SSRAM banks, flash, SD/MMC socket, and RS232 connectors.
	Lancelot VGA IP Design Kit **Microtronix Inc.**	Daughtercard	Kit includes a small hardware board with a 24-bit RAMDAC, VGA connector, stereo audio connector, and 2 PS/2 connectors.
	Compact Flash Expansion Kit **Microtronix Inc.**	Daughtercard	Inexpensive module allows the addition of compact flash cards to the Microtronix Product Starter Kit development board system.
General purpose	Cyclone III FPGA Starter Kit* [DK-START-3C25N] **Altera Corporation**	Cyclone III EP3C25N	1-Mbyte SSRAM, 16-Mbytes DDR SDRAM, 16-Mbytes parallel flash, configuration via USB, 4x user push buttons, 4x user LEDs, power measurement circuitry. Complete documentation including reference designs: *Create your first FPGA design in a hour*, *Measure Cyclone III FPGA power*. This kit also includes Quartus II Web Edition design software, evaluation edition of Nios processor plus related design suite, and Altera IP library.
	Cyclone II FPGA Starter Development Kit* [DK-CYCII-2C20N] **Altera Corporation**	Cyclone II EP2C20N	8-Mbit SDRAM, 512-Kbit SRAM, 1/4-Mbit flash, 24-bit audio CODEC, 10 switches, 4 push buttons, 4 7-segment displays, 10 red and 8 green LEDs, VGA, RS-232, and PS/2 ports, 2 40-pin expansion ports, SD/MMC socket.
	DB2C5 **EBV**	Cyclone II EP2C5	Provides an entry point into Altera's current FPGA technology. Three LVDS input channels and output channels are available for high-speed communication with other modules. Available I/O pins are connected with plugs on the underside of the board.
	DB2C20 **EBV**	Cyclone II EP2C20	FPGA-based development board designed specifically for Altera's Nios II embedded processors and the .NET Framework in the industrial market.
	DE2 Development and Education Board **Terasic Technologies Inc.**	Cyclone II EP2C35	Many high-end multimedia features (USB, CD-quality audio, DTV, Ethernet, SD, and LCD).

* RoHS compliant (lead free)

Development kits (continued)

General purpose (continued)

Product name and vendor name	Device	Features
Hpe Mini **Gleichmann Electronics Research**	Cyclone II EP2C35	An FPGA and ASIC system-on-a-chip (SOC) development tool with variants to create simplified or complex CPU systems.
ezFPGA Cyclone Prototyping & Evaluation Kit **Dallas Logic**	Cyclone EP1C3	Small prototyping module, designed specifically for quick project integration.
DB1C6 **EBV**	Cyclone EP1C6	Low-cost Cyclone FPGA development board providing a hardware platform for a wide range of applications.
DB1C12 USBB **EBV**	Cyclone EP1C12	Development board for industrial communication solutions. Provides enough resources for complex Nios II designs with several communication channels.
Altium Designer LiveDesign Evaluation Kit **Altium**	Cyclone EP1C12	Provided with a versatile low-cost, FPGA-based development board featuring a high-capacity Altera Cyclone FPGA.
Twister DDR SDRAM Evaluation Kit **AleaREP**	Cyclone EP1C6	An evaluation board for exploring DDR SDRAM memory along with Altera's low-cost Cyclone devices, this evaluation kit is ideal for existing Nios embedded processor users, kit owners, and developers who require additional memory bandwidth, or intend to use low-cost DDR memories.
Hpe Compact **Gleichmann Electronics Research**	Stratix II EP2S60 to EP2S180	An FPGA and ASIC development tool providing a low-cost environment for creating complete system development.
RUBY II PMC Prototyping Board **ReFLEX CES**	Stratix II EP2S60 to EP2S180	PCI mezzanine card (PMC) prototyping board supporting Stratix II devices in FPGA 1020 pin packages.
TREX S2 Prototyping System **Terasic Technologies Inc.**	Stratix II EP2S60 or EP2S180	700 available user I/O pins, flexible and reusable, a selection of various motherboards, high-speed connectors to enable DDR2 memory access.
Stratix II Demo Board **Galaxy**	Stratix II EP2S180	Designed for IC development and verification, compatible with Altera Stratix II 1020 device family.
PM480 Dual Channel ADC PMC **Parsec**	Stratix EP1S10 to EP1S30	Dual ADC PMC module, 150 MSPS 14-bit ADCs, wideband IF sampling, multi-channel receiver, radar, SDR, Windows and MATLAB driver, DDC reference design.
PM488 Dual Channel DAC PMC Module **Parsec**	Stratix EP1S10 to EP1S30	Dual DAC PMC module, 150 MSPS 14-bit DACs, base band or IF generation, radar, SDR, wireless basestations, Windows and MATLAB driver.
TS PCI A25 General Purpose Development Kit **GE Fanuc**	Stratix EP1S25	General-purpose mezzanine I/O, wave FPGA software tool kit, Quartus II design software, SOPC Builder, and Nios II evaluation edition software, documentation, and cables.
TS PCI 104 General Purpose Development Kit **GE Fanuc**	Stratix EP1S40	When combined with SOPC Builder, Avalon® bus architecture, and Nios II soft-core processor package, allows for a flexible and scalable architecture for FPGA development.
DIGILAB SX High-End Prototyping System **El Camino GmbH**	Stratix EP1S30 to EP1S80	Board includes 2 SODIMM connectors, 2 Santa Cruz connectors, optional SSRAM/flash memory modules available.
DB1270 **EBV**	MAX II EPM1270	Low-cost MAX II CPLD development board providing a hardware platform for a wide range of applications.
MAX II Starter Kit **Galaxy**	MAX II EPM1270	Kit can also be used by designers interested in simulating and synthesizing programmable logic circuits in their applications.
MAX II Development Kit* [DK-MAXII-1270N] **Altera Corporation**	MAX II EPM1270N	USB MAC/PHY, PCI Edge connector (3.3- and 5-V tolerant), LCD module, SRAM (128K x 8 bit), temperature gauge with serial peripheral interface (SPI), onboard power meter, active I/O sense circuitry, expansion/prototype header, four switches, four LEDs.
DBMAXLED **EBV**	MAX II EPM1270	Demonstrates that a single MAX II EPM1270 device can drive a large number of PWM channels.

* RoHS compliant (lead free)

Development kits (continued)

General purpose (continued)

Product name and vendor name	Device	Features
DIGILAB picoMAX Prototyping Board and Starter Kit **El Camino GmbH**	MAX EPM3032A to EPM7160S	MAX 3000/MAX 7000 starter kit, includes download/ programming hardware.
DB3128 **EBV**	MAX EPM3128A	Low-cost MAX 3000A CPLD development board with 128 macrocells, providing an easy entry point into Altera's CPLD technology.
DB3256 **EBV**	MAX EPM3256A	Low-cost MAX 3000A CPLD development board with 256 macrocells, providing an easy entry point into Altera's CPLD technology.
PM410 StarFabric Compact PCI Carrier Board **Parsec**	MAX EPM3256A	Two 3.3-V PMC sites, 32/64-bit 33/66 MHz PCI busses, 2.5-Gbps StarFabric links on J3, supports full PCI bandwidth.
TRDB_DC2 1.3 Megapixel Camera Module **Terasic Technologies Inc.**	Daughtercard	Complete digital camera reference design with source code in Verilog HDL, user manual with live demo examples; supports exposure, light-controlling, and motion capturing.
TRDB_LCM Digital Panel Daughtercard **Terasic Technologies Inc.**	Daughtercard	3.6" digital panel development kit, reference designs (TV player and color pattern generator) with source code in Verilog HDL.
ASIC prototyping		
PROC2S Stratix II FPGA Board **GiDEL Limited**	Stratix II EP2S60 to EP2S180	Functions as ASIC replacement in customer prototyping environment.
PROCStar II Development Kit **GiDEL Limited**	Stratix II EP2S60 to EP2S180 (1 - 4 devices)	Provides a high-capacity, high-speed FPGA-based platform.
MAGMA High-Speed Prototyping Board **ReFLEX CES**	Stratix II EP2S180	High-speed prototyping board featuring four high-density FPGA devices.
HAC2 **Gleichmann Electronics Research**	Stratix II EP2S180	A hardware accelerator and cosimulator development tool with key features such as high-speed clock acceleration and hardware-in-the-loop for rapid system exploration.
DNMEG S2GX Stratix II GX Based ASIC Prototyping Kit **The DiNi Group**	Stratix II GX daughtercard	A logic emulation daughtercard enabling ASIC or IP designers to cost effectively prototype logic and memory designs.
DN5000K10 Stratix-Based ASIC Prototyping Kit **The Dini Group**	Stratix EP1S40 to EP1S80	A logic emulation system enabling ASIC or IP designers to cost effectively prototype logic and memory designs.
PROCSuperStar Stratix 80 Board **GiDEL Limited**	Stratix EP1S80	An expandable, building-block type system enabling up to 21 Stratix EP1S80 FPGAs to be used on the board.
DN5000K10S Stratix-Based ASIC Protyping Kit **The Dini Group**	Stratix EP1S80 (2-5 devices)	A logic emulation PWB using the BG1508 package.

* RoHS compliant (lead free)

FOR MORE INFORMATION

Development kits **www.altera.com/devkits**

Training

Attend an Altera technical training course to reduce your time-to-market and achieve optimal design results. Our courses give you the skills you need to quickly produce high-performance, small-footprint designs.

Altera instructor-led training courses *(All courses are one day in length unless otherwise noted)*

Course category	General description	Course titles
Design languages	Attain the skills needed to design with Verilog HDL and VHDL for programmable logic.	• Introduction to VHDL • Advanced VHDL Design Techniques • Introduction to Verilog HDL • Advanced Verilog HDL Design Techniques
Software	Acquire design entry, compilation, programming, verification, and optimization skills by learning how to use both basic and advanced features of Quartus II software.	• Quartus II Software Design Series: Foundation • Quartus II Software Design Series: Verification • Quartus II Software Design Series: Optimization
FPGA	Create optimal FPGA designs by learning design techniques that take advantage of key device features and resources.	• Designing with Stratix II Devices • Designing with Stratix III Devices
Structured ASICs	Create optimal structured ASIC designs using an FPGA as a prototyping vehicle. Learn design techniques that take advantage of key device features and resources.	• Designing with HardCopy II Devices
Embedded systems	Learn to design a Nios II soft-core microprocessor system in an Altera FPGA and increase software execution speed through hardware acceleration.	• Designing with the Nios II Processor and SOPC Builder (for hardware engineers) • Developing Software for the Nios II Processor (Course length: two days; for software engineers) • Implementing Embedded Systems with Programmable Logic • Accelerating Software Using the Nios II C2H Compiler
High-speed	Implement high-speed I/O protocols using FPGA multigigabit transceivers. Take advantage of the architecture, operating modes, and features discussed throughout the course to optimize your design. Gain understanding of the fundamentals of signal integrity in high-speed design.	• High-Speed Design Using Stratix II GX Devices (Course length: two days)
DSP	Solve DSP design challenges using Altera technology and the skills you will learn in these classes.	• Implementing DSP Designs in FPGAs • Advanced DSP Design: Using FPGAs to Architect and Optimize a Communication System • Advanced DSP Design: Using FPGAs to Architect and Optimize a Video and Image Processing System

Online offerings

Online classes give you an overview of a variety of features and design techniques. Take advantage of these free, online training modules to preview topics covered in greater depth in our instructor-led classes, brush up on key how-to tips, or even jump-start your design.

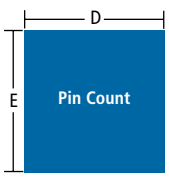
Altera instructor-led training courses *(All courses are one day in length unless otherwise noted)*

Course category	Course titles
Design languages	• VHDL Basics • Verilog HDL Basics
Software	• Using Quartus II Software: An Introduction • Design Planning Guidelines for High-Density FPGAs • Using Quartus II Software: Schematic Design • Using Quartus II Software: Timing Analysis • Using Quartus II Software: Simulation • Validating Performance With the TimeQuest Static Timing Analyzer • Switching to the TimeQuest Timing Analyzer • Constraining and Analyzing Timing for Source Synchronous Circuits with TimeQuest • Introduction to Incremental Compilation • Incremental Compilation for Team-Based Designs • Using Quartus II Software: Incremental Compilation • Design Debugging Using the SignalTap II Logic Analyzer • SignalTap II Logic Analyzer: New Features in Quartus II 6.0 • Using Quartus II Software: Managing Design Changes With Chip Editor • Using Quartus II Software: Chip Planner • I/O Management • Power and Thermal Management • PowerPlay Power Analyzer Tool in Quartus II Software • PowerPlay Power Analyzer Tool (Quartus II 6.0 Update) • FPGA to Board Design Flow Using Mentor Graphics Tools • Signal Integrity Analysis with Third-Party Tools
Devices	• Stratix III Devices: Features and Capabilities • Using Stratix and Stratix II High-Speed Design Features • Cyclone III Devices: Features and Capabilities • HardCopy II Design Flow in Quartus II Software • Implementing HardCopy II Structured ASIC Timing Constraints in Quartus II Software
Applications	• Using DSP Builder • Using SOPC Builder • System-on-a-Programmable-Chip Design Using the Nios II Embedded Processor • Nios II C2H Compiler Fundamentals • Nios II Floating Point Custom Instructions • Using the sld_virtual_jtag (VJI) Megafunction • Viterbi Decoder • Using Cascaded-Integrator-Comb Filter in Multirate Digital Systems

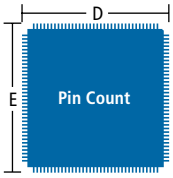
FOR MORE INFORMATION Training www.altera.com/training

Package dimensions

Legend



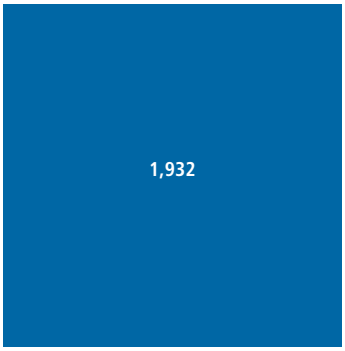
D (mm) x E (mm)
Pitch (mm)



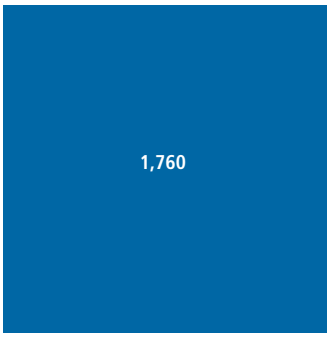
D (mm) x E (mm)
Pitch (mm)

Note: Outermost dimensions are "D" and "E" for both array and peripheral package families

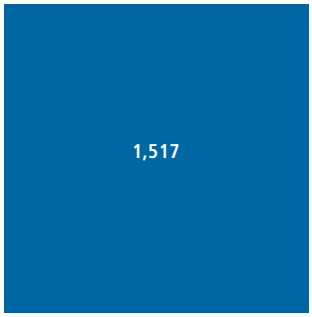
FineLine BGA (FBGA) and Hybrid FineLine BGA (HFBGA)



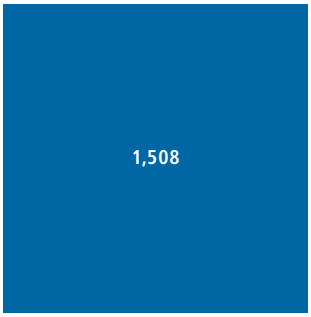
45.00 x 45.00
1.00



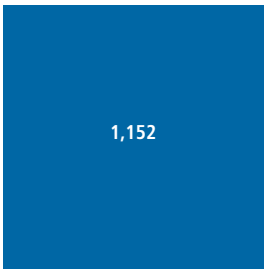
43.00 x 43.00
1.00



40.00 x 40.00
1.00

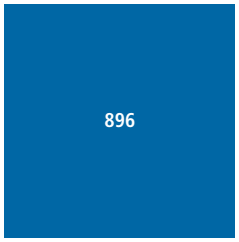


40.00 x 40.00
1.00

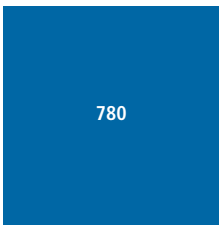


35.00 x 35.00
1.00

33.00 x 33.00
1.00



31.00 x 31.00
1.00



29.00 x 29.00
1.00

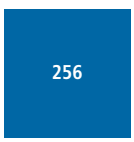
27.00 x 27.00
1.00

27.00 x 27.00
1.00

23.00 x 23.00
1.00

21.00 x 21.00
1.00

19.00 x 19.00
1.00



17.00 x 17.00
1.00

13.00 x13.00
1.00

11.00 x 11.00
1.00

Micro FineLine BGA (MBGA)

256: 11.00 x 11.00, 0.50

100: 6.00 x 6.00, 0.50

Ultra FineLine BGA (UFBGA)

484: 19.00 x 19.00, 0.80

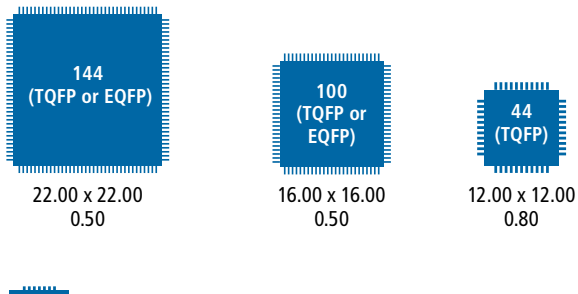
256: 14.00 x 14.00, 0.80

169: 11.00 x 11.00, 0.80

88: 11.00 x 8.00, 0.80

49: 7.00 x 7.00, 0.80

Thin Quad Flat Pack (TQFP), Enhanced Thin Quad Flat Pack (EQFP)



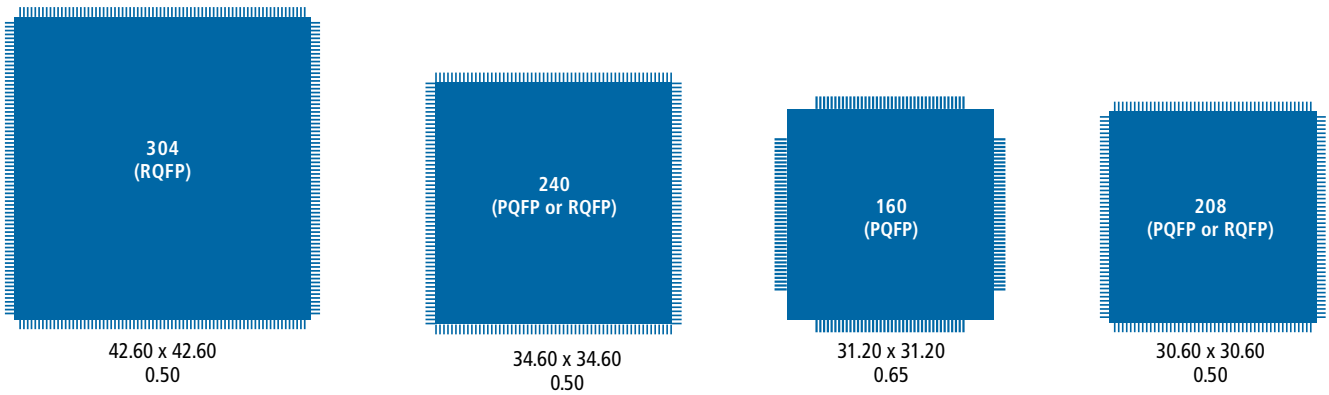
144 (TQFP or EQFP): 22.00 x 22.00, 0.50

100 (TQFP or EQFP): 16.00 x 16.00, 0.50

44 (TQFP): 12.00 x 12.00, 0.80

32 (TQFP): 9.00 x 9.00, 0.80

Plastic Quad Flat Pack (PQFP), Power Quad Flat Pack (RQFP)

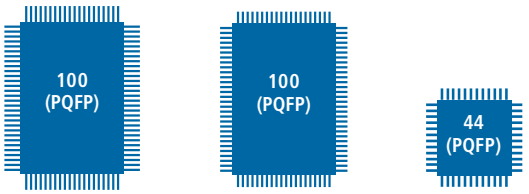


304 (RQFP): 42.60 x 42.60, 0.50

240 (PQFP or RQFP): 34.60 x 34.60, 0.50

160 (PQFP): 31.20 x 31.20, 0.65

208 (PQFP or RQFP): 30.60 x 30.60, 0.50

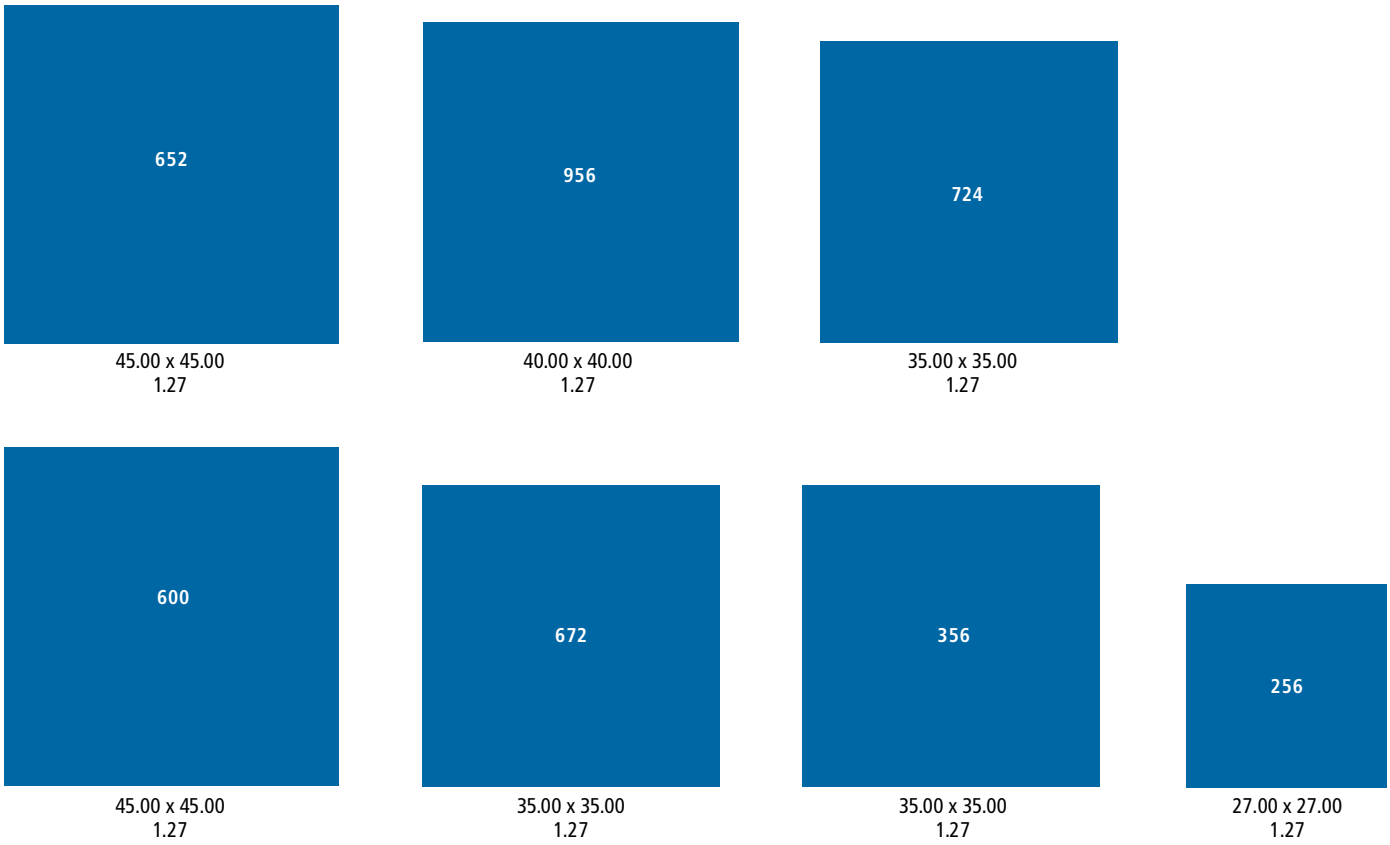


100 (PQFP): 18.30 x 24.30, 0.65, (EPC8 and EPC16)

100 (PQFP): 17.20 x 23.20, 0.65

44 (PQFP): 13.20 x 13.20, 0.80

Ball-Grid Array (BGA)



Ordering codes

Family Signature

EPM: MAX 7000, MAX 3000

Device Type

7032S, 7064S, 7128S, 7160S, 7192S, 7256S, 7032AE, 7064AE, 7128AE, 7256AE, 7512AE, 7032B, 7064B, 7128B, 7256B, 7512B, 3032A, 3064A, 3128A, 3256A, 3512A

Package Type

B: Ball-grid array (BGA)
F: FineLine BGA (FBGA)
L: Plastic J-lead chip carrier (PLCC)
Q: Plastic quad flat pack (PQFP)
R: Power quad flat pack (RQFP)
T: Thin quad flat pack (TQFP)
U: Ultra FineLine BGA (UFBGA)

Operating Temperature

C: Commercial temperature (0° C to 90° C)
I: Industrial temperature (-40° C to 105° C)

Pin Count

Number of pins for devices with different pin-count options

Speed Grade

See the current individual device family data sheet for speed/product relationships (e.g.,-4, -7, -10)

Optional Suffix

Indicates specific device options or shipment method
F: Fixed programming algorithm
H: Special dry-packaging shipment option for MAX 7000 devices
P: Special PCI compliance on selected devices
T: MAX devices with different timing specifications
N: Lead-free

EP1S	25	F	780	C	5	N

Family Signature

EPM: MAX II
EP3C: Cyclone III
EP2C: Cyclone II
EP1C: Cyclone
EP1AGX: Arria GX
EP3SL: Stratix III L
EP3SE: Stratix III E
EP2S: Stratix II
EP2SGX: Stratix II GX
EP1S: Stratix
EP1SGX: Stratix GX
HC2: HardCopy II
HC1S: HardCopy Stratix

Device Type

EPM: 240, 570,1270, 2210
EP3C: 5, 10, 16, 25, 40, 55, 80, 120
EP2C: 5, 8, 8A, 15A, 20, 20A, 35, 50, 70
EP1C: 3, 4, 6,12, 20
EP1AGX: 20, 35, 50, 60, 90
EP3SL: 50, 70, 110, 150, 200, 340
EP3SE: 50, 80, 110, 260
EP2S: 15, 30, 60, 90, 130,180
EP2SGX: 30, 60, 90, 130
EP1S: 10, 20, 25, 30, 40, 60, 80
EP1SGX: 10, 25, 40
HC2: 10W, 10, 20, 30, 40
HC1S: 25, 30, 40, 60, 80

Transceiver Channels

For GX devices only
C: 4
D: 8
E: 12
F: 16
G: 20

Product-Line Suffix

For MAX II devices only
Indicates device core voltage
G: 1.8-V V_{CCINT} device
Blank: 2.5-V or 3.3-V V_{CCINT} device

Package Type

B: Ball-grid array
E: Enhanced thin quad flat pack
F: FineLine BGA
H: Hybrid FineLine BGA (HFBGA)
M: Micro BGA
T: Thin quad flat pack
U: Ultra FineLine BGA
Q: Plastic quad flat pack

Pin Count

Number of pins for devices with different pin-count options

Operating Temperature

C: Commercial temperature (0° C to 85° C)
I: Industrial temperature (-40° C to 100° C)

Speed Grade

	Fast ← → Slow						
	2	3	4	5	6	7	8
MAX II		✓	✓	✓			
Cyclone III					✓	✓	✓
Cyclone II					✓	✓	✓
Cyclone					✓	✓	✓
Arria GX					✓		
Stratix III L	✓	✓	✓				
Stratix III E	✓	✓	✓				
Stratix II		✓	✓	✓			
Stratix II GX		✓	✓	✓			
Stratix				✓	✓	✓	
Stratix GX				✓	✓	✓	

Optional Suffix

Indicates specific device options or shipment method
ES: Engineering sample
N: Lead free

Product websites and information

MAX CPLD series

MAX II CPLDs
www.altera.com/max2

MAX 3000A CPLDs
www.altera.com/products/devices/max3k

MAX 7000 CPLDs
www.altera.com/products/devices/max7k

Cyclone low-cost FPGA series

Cyclone III FPGAs
www.altera.com/cyclone3

Cyclone II FPGAs
www.altera.com/cyclone2

Cyclone FPGAs
www.altera.com/cyclone

Arria GX low-cost FPGA family

Arria GX FPGAs
www.altera.com/arriagx

Stratix high-end FPGA series

Stratix III FPGAs
www.altera.com/stratix3

Stratix II FPGAs
www.altera.com/stratix2

Stratix II GX transceiver FPGAs
www.altera.com/stratix2gx

Stratix FPGAs
www.altera.com/stratix

Stratix GX transceiver FPGAs
www.altera.com/stratixgx

HardCopy structured ASIC series

HardCopy structured ASIC series
www.altera.com/hardcopy

HardCopy II structured ASICs
www.altera.com/hardcopy2

HardCopy Stratix structured ASICs
www.altera.com/hardcopystratix

Nios II embedded processors

Nios II processors
www.altera.com/nios2

Nios user forum
www.niosforum.org

Nios II development kits
www.altera.com/nioskits

Nios II C2H Compiler
www.altera.com/c2h

Have comments about this catalog?
Email us at catalog@altera.com.

Intellectual property solutions

IP MegaStore
www.altera.com/ipmegastore

Quartus II design software

Quartus II software
www.altera.com/quartus2

Quartus II Web Edition and Subscription Edition download
www.altera.com/download

Purchase Quartus II software
www.altera.com/buysoftware

Quartus II literature
www.altera.com/literature

Development kits

Altera and partner development kits
www.altera.com/devkits

Training

Altera technical training
www.altera.com/training

Literature

More details on Altera and partner offerings
www.altera.com/literature

Notes

Notes

Notes

Notes

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
USA
Telephone: (408) 544-7000
www.altera.com

Altera European Headquarters
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1 494 602 000

Altera Japan Ltd.
Shinjuku I Tower 32F
6-5-1, Nishi Shinjuku
Shinjuku-ku, Tokyo 163-1332
Japan
Telephone: (81) 3 3340 9480
www.altera.co.jp

Altera International Ltd.
2102 Tower 6
The Gateway, Harbour City
9 Canton Road
Tsimshatsui Kowloon
Hong Kong
Telephone: (852) 2945 7000
www.altera.com.cn

30K May 2007 SG-PRDCT-4.0